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Impact of the etching time and current density on Capacitance-Voltage characteristics of P-type of porous silicon

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ABSTRACT

In This paper, electrochemical etching teqniques was using to formation of nano crystalline porous silicon layer on p-type Si substrates. Measurement of capacitance – voltage characteristics at various etching time and current densities were used for calculated built in voltage and type of heterojunction. The built in voltage values were decreased with increasing etching time and current densities for both anisotype Al/PS/p-Si/Al heterojunction. These characteristics are interpreted by assuming the abrupt heterojunction model. The effect of different etching time and current densities on electrical properties of PS have been investigated.

Keyword: porous silicon, electrochemical etching, thin films, heterojunction

1. INTRODUCTION

Porous silicon is a very promising material due to its excellent properties and compatibility with silicon based microelectronics with reduced fabrication cost [1]. Porous silicon PS has unique properties such as direct and wide modulated energy band gap, high resistivity, vast surface area-to-volume ratio and the same single-crystal structure as bulk Si [2]. Typically, the PS layer is sandwiched between the c-Si substrate and a metallic contact.

The PS layer was considered to behave like a wide band gap semiconductor and assumed a Schottky barrier formed between the metal and the PS [3]. Capacitance-voltage measurement is one of the most important methods for obtaining information about the rectifying junctions, built-in potential, and junction capacitance and junction type. Sometimes the capacitance under forward bias exceeds the space-charge capacitance predicted by theory. The excess capacitance is due to traps at the junction interface. These traps can be created by dangling bonds, inter-diffusion of atoms and crystal defects at the metal/semiconductor or organic materials/inorganic semiconductor interfaces [4].

The capacitance-voltage measurements of the junction are performed at different frequencies. The relation between voltage and capacitance can be expressed as equation [5]:

$$C_d = A\left[\frac{eN_d\varepsilon}{2(V_{bi}-V)}\right]^{1/2} \tag{1}$$

With the top and bottom metal electrodes, the parameters of the Schottky diode, including the depletion layer capacitance C_d , built-in voltage V_{bi} and space charge density ($N_D or N_A$) can be determined from a plot of 1/C (C is the measured capacitance) versus t (t is measured thickness), at various bias voltages .We assume that Schottky barriers are formed at the top and bottom interfaces . With built in voltageV_{bi}, a depletion width should follow a relationship such as:

$$W = [\frac{2\in_i\in_\circ}{qN_d}(V_{bi} - V)]^{0.5} \quad . \tag{2}$$

and

$$W = \sqrt{\frac{2\varepsilon V_{bi}}{qN_e}} \tag{3}$$

W is related with junction capacitance C as W = ε A/C where ε is permittivity and A is junction area, thus $d = \varepsilon_{PS}A/C_{PS}$ whereε_{ps} and c_{ps} are permittivity and junction capacitance of PS. The capacitance – voltage characteristics of PS/c-Si structure depend on the morphology and the porosity of the etched silicon surface, whereN_D, is the donor density, $\in_i$ is the relative permitivity of interfacial layer and $\in_\circ$ is the permittivity of vacuum [6].

The C-V measurements are made and are plotted as graphs of $1/C^2$ versus V (Volt). Due to nonlinearity of the slopes, calculations are made in the selected voltage range of 1-3 V. The built-in potential is obtained from the intersection of the f(V) = $1/C^2$ plot with the abscissa. According to capacitance-voltage measurements, drawing $1/C^2$ versus V does not give a straight line.

This means that the depletion layer and the barrier height are not constant and so the carrier concentration will not be constant at the depletion layer [7].In this work, we have fabricated porous silicon layers by using electrochemical etching (ECE) teqniques. The electrical properties of Al/PS Schottky as functions of the etching and etching current densities by measuring Capacitance-Voltage characteristics at room temperature was studied.

2. EXPERIMENTAL

2. 1. Electrochemical Etching

The fabrication of Porous Silicon (PS) is a comparatively simple process that only requires a small amount of equipment. The simplest cell which can be used to anodize silicon is shown in Figure 1.

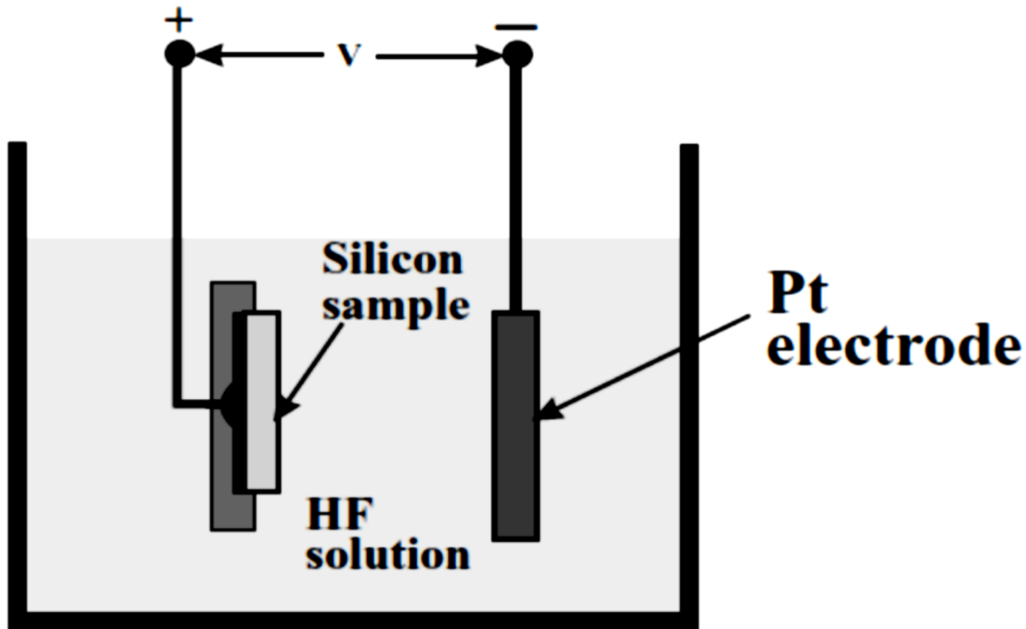

Fig. 1. Schematic of the designed porous silicon fabrication system [8]

The silicon wafer serves as the anode. The cathode is made of platinum or any HF-resistant and conducting material. The cell body itself is, in general, made of highly acid-resistant polymer such as Teflon. Since the entire silicon wafer serves as the anode, PS is formed on any wafer surface in contact with the HF solution, including the cleaved edges. The advantage of such equipment is its simplicity [9]. The main element of the system as shown electrochemical cell. We used this method to prepare PS from p-type as shown in the following sections.

2. 2. Preparation of samples

Porous silicon layers are produced using monocrystalline silicon wafers, p-type, with resistivity's ranging from (14-22) Ω·cm. The wafers Si (111) face orientation. Samples are made of porous silicon produced with a standard technique of anodizing silicon substrates in an electrolyte (40%) HF : (99.8%) CH_3OH with a volume ratio of [1:1] The Si wafer first cuts to 1×1 cm^2samples before cleaning. Cleaning is necessary to remove any traces of organic, metallic and ionic contaminants from samples. Methanol and alcohol are used commonly to clean the wafer by immersing it in these chemicals in turn in the ultrasonic bath for few minutes. Finally, they are rinsed in distilled water treated ultrasonically followed by drying in

a hot air stream. To ensure as uniform a current distribution as possible, the samples are coated with ≈800 nm layer of aluminum on the backside. The samples are prepared in sandwich configuration, top Al/PS/c-Si/bottom Al, the top one semitransparent electrode thermally evaporated with 78nm and the bottom electrode is coated with ~ 800 nm Aluminum layer before the anodization process. Porous silicon (PS) samples are prepared by anodization in HF: and CH_3OH (1:1) solution at a constant current density (values within the range from 20 mA/cm² -60 mA/cm²) for different times to any value of current density (5 min – 40 min).

2. 3. Metallization

Metallization on PS has also become another important area of interest, especially in the Schottky diode structure. The success of PS in the application areas depends on how the big challenge in seeking suitable metallization can be overcome [10]. The evaporation is performed in a vacuum pressure of 10^{-6} torr, using an evaporation plant model "E306 A manufactured by Edwards high vacuum". After the evaporation process, the thickness of evaporated film on a glass substrate is measured using gravimetric method. The thickness measurement by gravimetric method is curried out using the equation:

$$m = 2\rho\pi l^2 t \tag{4}$$

where m is the net mass of evaporated Al on glass substrate, $\rho = 2.7 g.cm^{-3}$ and l = 15 cm the distance between the boat and substrate. The samples are prepared in sandwich configuration, top Al/PS/c-Si/bottom Al, the top one (Al) semi-transparent electrode thermally evaporated thin layer. The rear-side ohmic contacts were fabricated by the electro-chemical deposition of thick Al film to get sandwich structure as shown in cross section of Al/PS/p-Si/Al of Figure 2.

Figure 2. Cross-sectional view of Al/PS/p-Si/Al metal semiconductor metal structure

3. RESULTS AND DISCUSSION

The capacitance-voltage characteristic and the corresponding C^{-2} curve are shown in following Figures (4-7). The built-in voltage is obtained at the intersection of them C^{-2} curve and the horizontal axis. Figures (3-7) show the (C–V) and $(C^{-2} - V)$ measurements of the

PS/c-Si heterojunction in dark at room temperature and at the increment voltage of frequency 200 kHz. This result shows that the junction capacitance is inversely proportional to the bias voltage for the most of prepared samples. The C-V characteristics of the prepared device depend on the morphology and the porosity of the etched Si surface since it depend on etching time and current density as shown in (3-4) for p-typ.

The value of the built-in potentials for all PS/c-Si HJ and different etching time, current density for the prepared junction has been obtained and it has been found to have different values depending on the properties of the prepared device since it represents the energy required by the electron to transfer from the c-Si to PS. There was a decrease in the capacitance at strong bias and this reduction in the capacitance may be attributed to the increased conductivity at strong dc bias.

The linearity of this dependence indicates that the junction is reasonably interpreted by assuming an abrupt heterojunction. This property gives an indication of the behavior of the charge transition from the donor to the acceptor region, which is found to be "abrupt", this means that the depletion layer is constant and hence the carrier concentration will be constant at the depletion layer given in the most of Figures (3-7), but the depletion layer and the barrier height are not constant and so the carrier concentration will not be constant at the depletion in these Figures (7-A, B and C) since the drawing C^{-2} versus V does not give a straight line .These results are in good agreement with [11].

The reduction in the junction capacitance with increasing the bias voltage results from the expansion of depletion layer with the built-in potential. The width of the depletion layer $W_D$of the porous layer depends on concentration N_D, and the built-in potential (V_{bi}) according to equation:

$$W = [\frac{2\epsilon_i\epsilon_\circ}{qN_d}(V_{bi} - V)]^{0.5} \tag{5}$$

Therefore, any change in the concentration $N_D$will change the depletion layer width. As the etching current increases the pore size increases as well as the depletion layer width, thickness and resistance. This can be explained as the variation in the values of the built in voltage in Tables 1.

Table 1. Built in voltage V_{bi} as function on Current density and Etching time for PS/c-Si HJ.

Etching time (min)	**5**	**10**	**20**	**30**	**10**	**10**	**5**	**10**	**20**	**30**	**40**	**10**
Current density (mA/cm^2)	**20**	**20**	**20**	**20**	**30**	**40**	**50**	**50**	**50**	**50**	**50**	**60**
Built in voltage V_{bi} (v)	**0.5**	**2**	**1**	**0.75**	**…**	**…**	**1.5**	**2.4**	**0.35**	**…**	**0.45**	**---**

According to the C-V measurements, we can assume that the resulting junction is one-sided junction and extends in the silicon substrate side due to the depletion process in the porous layer [12]. It is known that a capacitance of a Schottky diode can be represented by Eq.5. It predicts a linear relationship between (C^{-2}) and V under strong bias conditions. The carrier doping density (N_d) values used in the calculations are determined from the slope of the linear part plot of C^{-2} vs. V curves. The following Figures (3-7) give the C-V and C^{-2} -V measurements for both junctions at optimum etching current density. Figure (3) demonstrate the variation of the junction capacitance versus reverse bias voltage at four different Etching Times (5, 10, 20, and 30) min with (20 mA/cm^2) current-density for p - type.

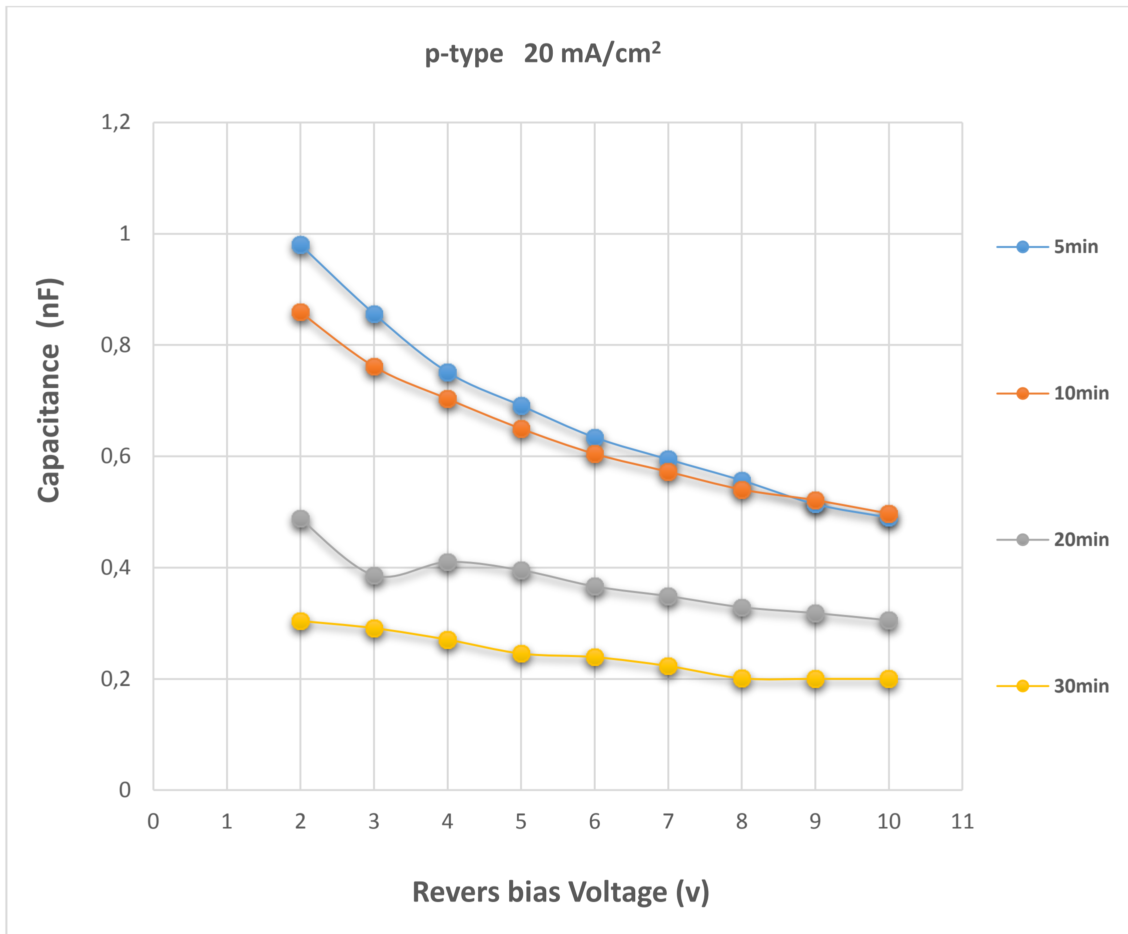

Fig. 3. Junction cpacitance of PS/p-Si HJ vs. the applied voltage at different etching time.

Figures (4) demonstrate the variation of the junction capacitance versus reverse bias voltage at four different Etching current density (20-60 mA/cm^2) with 10min etching time for p-type.

The junction capacitance is constant at (30 mA/cm^2 and 40 mA/cm^2), this indicate the non abrupt heterojunction PS/p-Si that agrees with our results in Figures (5-6). From the capacitance voltage measurements of the PS/p-Si heterojunction, by plotting the reciprocal squared of the junction capacitance against the applied reverse voltage, built-in potential ($\boldsymbol{V_{bi}}$).

The voltage intercepts of the extrapolated straight lines along the voltage axis are (0.5 - 2.5) V corresponding to the devices in p-type. Reduction of junction capacitance with increasing bias voltage is as a result of increasing depletion width. These characteristics are interpreted by assuming the abrupt heterojunction model.

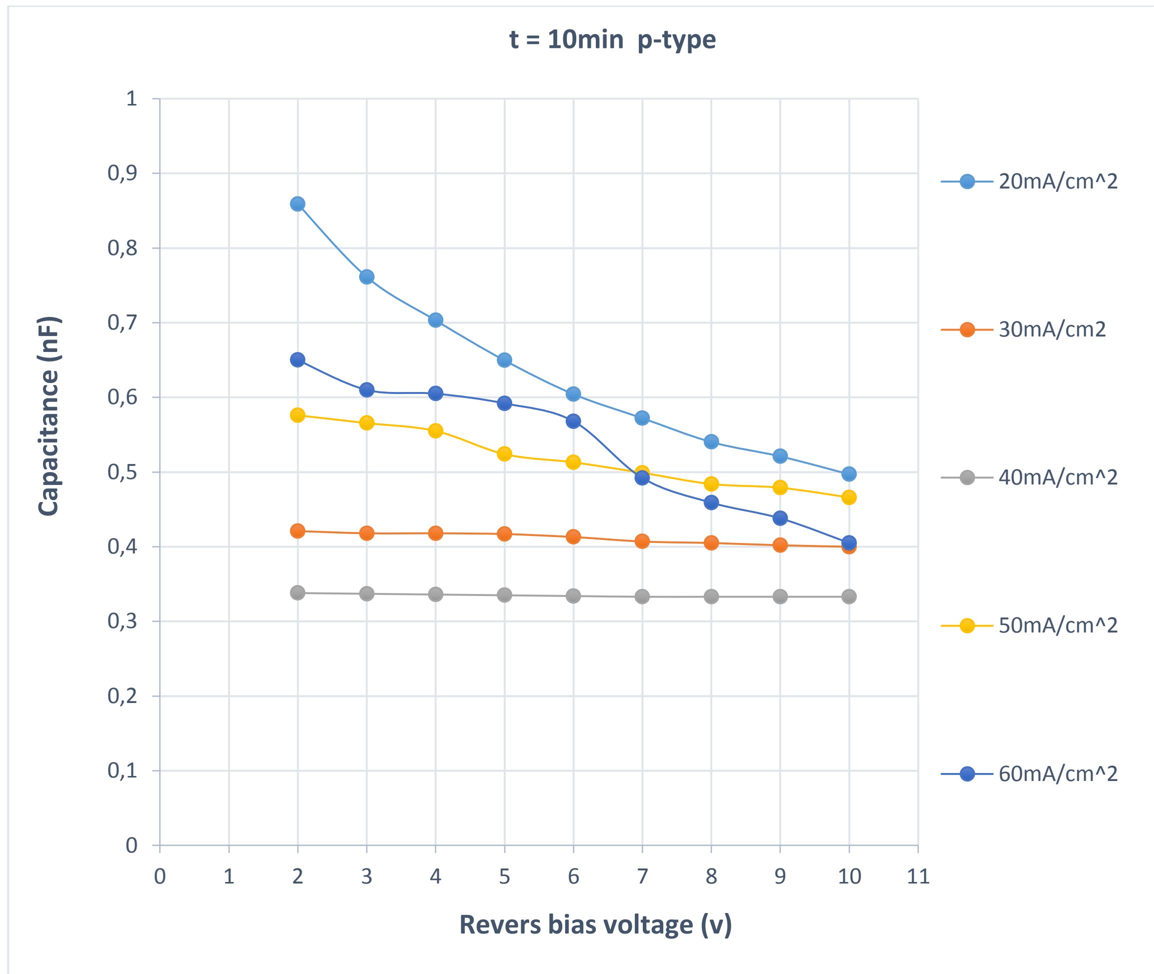

Fig. 4. Junction cpacitance of PS/p-Si HJ vs. the applied voltage at different density current.

C^{-2} versus V does not give a straight line. This means that the depletion layer and the barrier height are not constant and so the carrier concentration will not be constant at the depletion layer.

Table 1 also shows the effect of current-density and etching time on built in voltage for PS/p-Si and PS-n-Si heterojunction. It is obvious that V_{bi} reduces with rising etching time of (10-30) min for both anisotype Al/PS/p-Si/Al heterostructure. Also we show decreasing of built in voltage with increasing current-density at (30, 40, 50 mA/cm^2) for constant etching time 10 min. The built in voltage results presented in this work is in good agreement with those published by other authors [13-16].

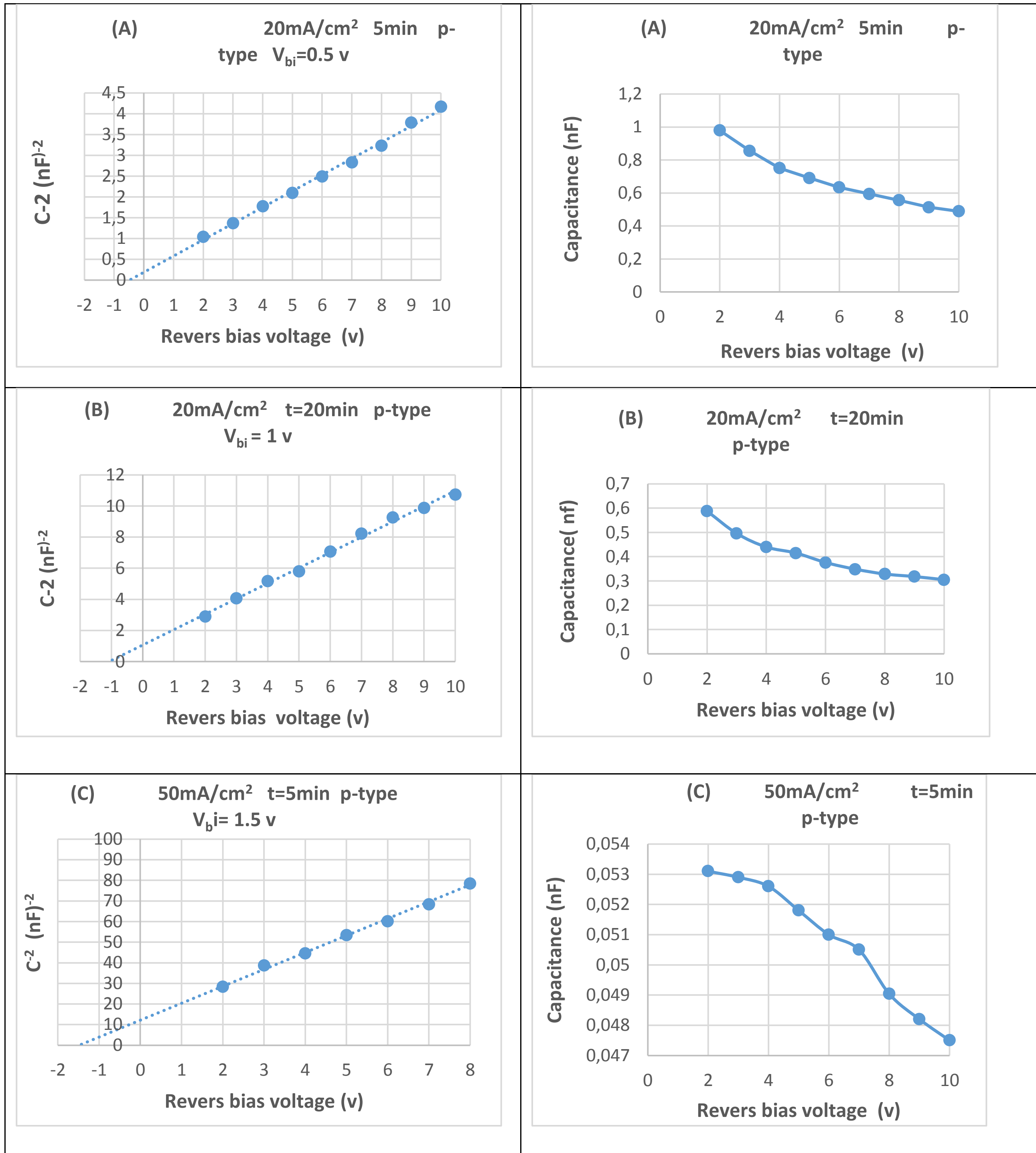

Fig. 5. (A, B and C). C^{-2} and Junction cpacitance of PS/p-Si HJ vs. the applied voltage at $20\ mA/cm^2$ - (5 and 20) min and $20\ mA/cm^2$ for 5 min respectivly.

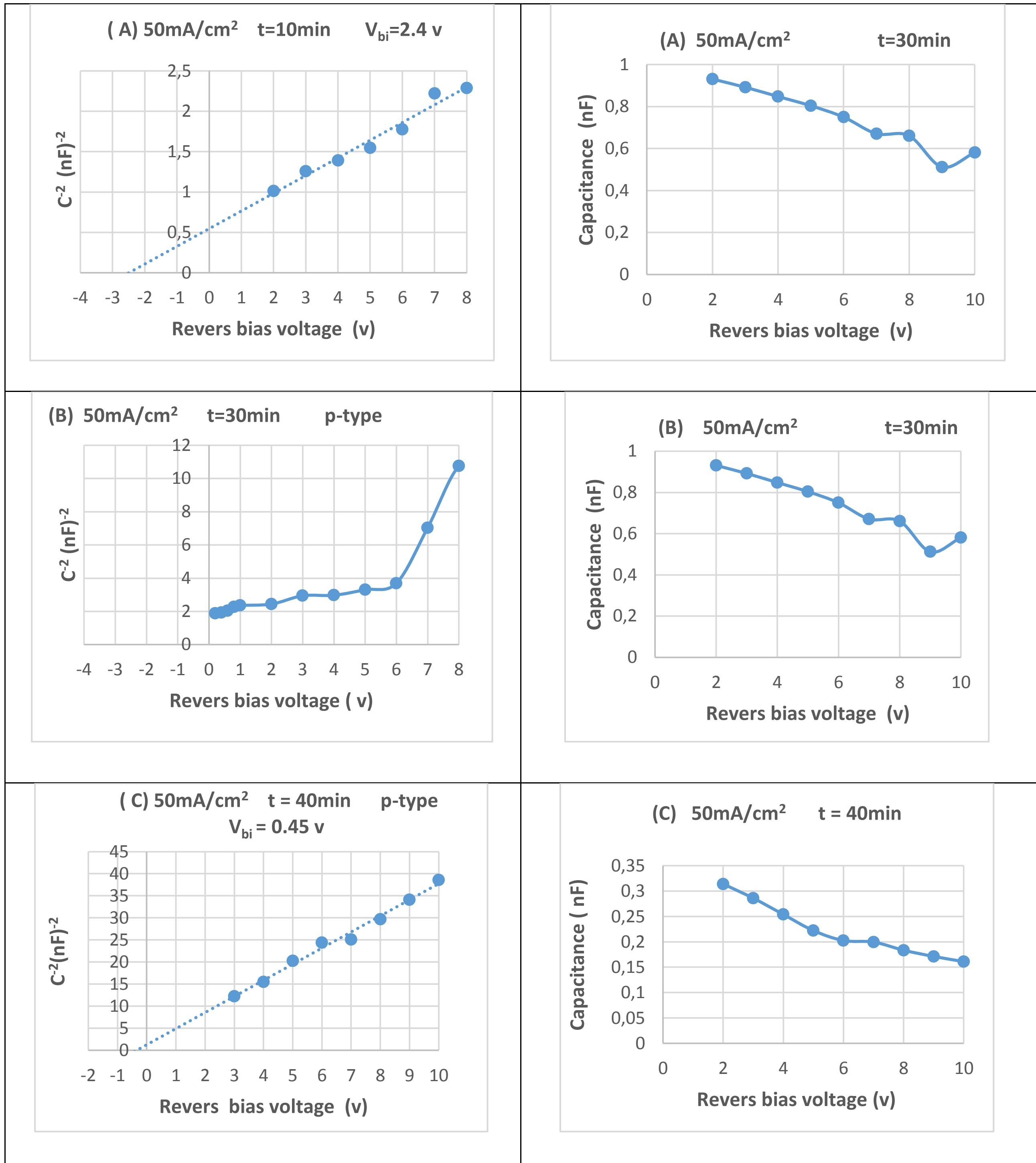

Fig. 6 (A, B and C). C^{-2} and Junction cpacitance of PS/p-Si HJ vs. the applied voltageat for $50\ mA/cm^2$ etching current density at different etching time (10, 30-40) min

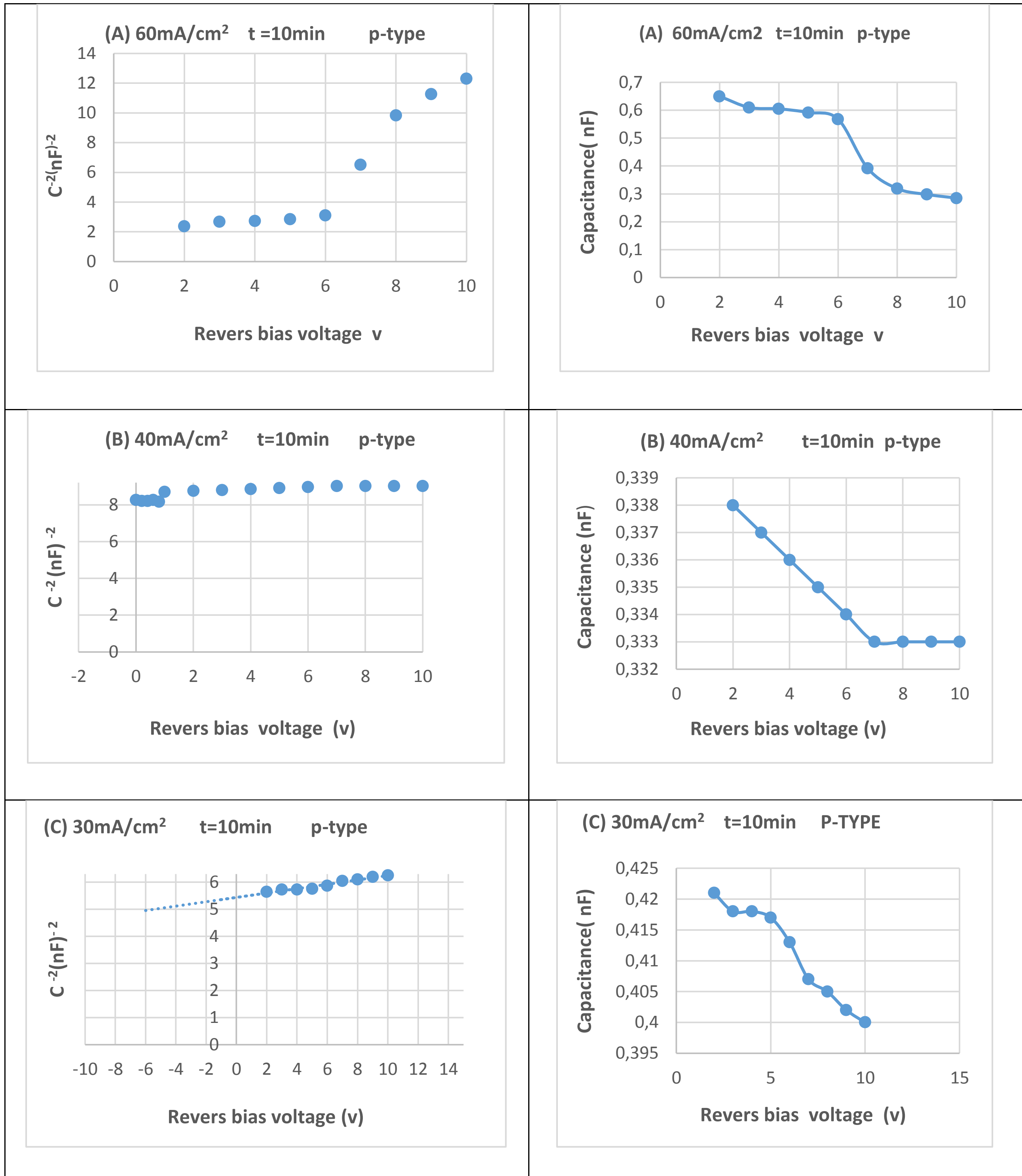

Fig. 7 (A, B and C): C^{-2} and Junction cpacitance of PS/p-Si HJ vs. the applied voltageat for $30{,}40 - 60\ \mathrm{mA/cm^2}$ etching current densities at 10 min etching time.

4. CONCLUSION

In this study, to examine the effect of etching time and etching current densities on the capacitance – voltage measurements at room temperature and we have calculated the values of built in voltage of aluminium / porous silicon / p-Si structures.

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