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Temperature dependent electrical characteristics of Nichrome/4H-SiC Schottky barrier diodes

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ABSTRACT

Nichrome Schottky barrier diodes have been fabricated on 4H-SiC substrates to investigate the temperature dependant electrical characteristics of the fabricated contacts. The electrical parameters such as barrier height, ideality factor and donor concentration were found from the current-voltage (I-V) and the capacitance-voltage (C-V) measurements at room temperature. Barrier Contacts showed non-ideal behaviour like lower value of barrier height and high value of ideality factor. A barrier height of 1.53eV obtained from C-V measurements and 0.79eV obtained from the I-V measurements with ideality factor of 1.96 for as-deposited diodes at room temperature. The diodes, therefore, were annealed in the temperature range from 25-400 ºC to see the effect of annealing temperature on these parameters. Schottky barrier height (SBH) and ideality factors were found temperature dependent. After rapid thermal annealing (RTA) upto 400 ºC barrier height of 1.27 eV from C-V measurements and the value of 1.13 eV were obtained from I-V measurements with ideality factor of 1.12. Since barrier height deduced from C-V measurements were consistently larger than those from I-V measurements. To remove this discrepancy we re-examined our results by including the effect of ideality factor in the expression of the saturation current. The insertion of ideality factor results in comparably good agreement between the values of barrier height derived by above two methods. We believe that the enhancement in the electrical parameters result from the improvement in the quality of interfacial layer.

***Keywords*:** Nichrome, Schottky Diodes, Schottky barrier height, ideality factor, rapid thermal annealing

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1. INTRODUCTION

Silicon Carbide (SiC) is one of the most promising wide band gap semiconductors, for future power devices. This is mainly due to its intrinsic properties such as high breakdown field strength, high saturated electron drift velocity, reasonable electron mobility and a very high thermal conductivity [1-3]. In recent years, significant progress has been made in the development of SiC power devices and most of the work has been done in the improvement of SiC (electronic devices, mainly) Schottky diodes due to their technological importance. Although SiC Schottky diodes are available commercially in the market, studies related to their properties and applications still remains important topic in today's research. A large number of workers have investigated the properties of SiC Schottky diodes both on 6H-SiC [4-9] and 4H-SiC [10-17]. More recently, investigators have shown interest in 4H-SiC, mainly due to its superior electrical properties such as the bandgap, high electron mobility and more isotropic nature compared to the other polytypes of SiC. [18]. Several studies related to SiC Schottky contacts have been carried out during the last two decades but the current transport and the temperature dependence of the barrier height in 4H-SiC Schottky diodes remains a subject of current interest. SiC SBD are mostly found to show non-ideal I-V-T characteristics and as a result they exhibit anomalous deviations in barrier height (ϕ_B) and ideality factor (n) with respect to temperature [19]. A large amount of published data is available on 4H-SiC Schottky diodes with different metal contacts like Ni, Ti, Au, Cr, Pt, Al, W, Mo, Cu, etc. Since ohmic contact on 4H and 6H-SiC using Nichrome shows more stability [20] than the nickel contacts, so in this work we report on Nichrome/4H-SiC Schottky diode. However, to our knowledge there is little information available on barrier height and ideality factor value with respect to rapid thermal anneal. The main objective of this paper is to investigate the effect of rapid thermal annealing on the electrical characteristics of Nichrome/4H-SiC Schottky contacts. Moreover the barrier heights deduced from CV measurements have been found consistently larger than those deduced from I-V measurements [12]. The reason behind this discrepancy has not been explained as yet. We have shown that the two sets of barrier height can be brought into close agreement when ideality factor is also included in the expression of the barrier heights.

2. DIODE FABRICATION AND CHARACTERIZATION

The starting material used for device fabrication was n-type 4H-SiC (001), 8º off Si face epiwafers purchased from Cree Inc. The substrate was n+-type with a donor concentration of 1×10^{18} cm^{-3} with a lightly doped ($N_D = 9\times10^{14}$ cm^{-3}) n-type epi-layer having specific resistivity of 0.020 Ωcm and thickness of 10 μm. Prior to metal deposition, the samples were degreased in organic solvents acetone, trichloroethylene and methanol successively. Immediately after degreasing, the samples were immersed in HF for 20 s at room temperature followed by rinse in DI water and blown dry. The back-side ohmic contacts were formed by deposition of nickel which was annealed in N_2 atmosphere at 900 °C for 10 min. Schottky contacts were deposited using Nichrome on 4H–SiC epilayer by e-beam metallization process at a pressure maintained between 1×10^{-6} to 1×10^{-7} Torr. The contact metal had a circular geometry with diameter of 1mm and typical thickness of 200 nm. Schematic of the diode is shown in Fig. 1. The forward current-voltage (I-V) characteristics were measured at room temperature for as-deposited as well as for annealed contacts using Keithley model 236 Source Measure Unit (SMU) in voltage range from 0-3V. The capacitance-voltage (C-V) characteristics were measured using Agilent LCR meter at frequencies of 1 MHz and 100 kHz with a dc voltage sweep of −5 to 0V. In order to obtain more insight into the current transport mechanism rapid thermal annealing was performed in nitrogen ambient for 20 minutes at temperature ranging from 25-400 ºC.

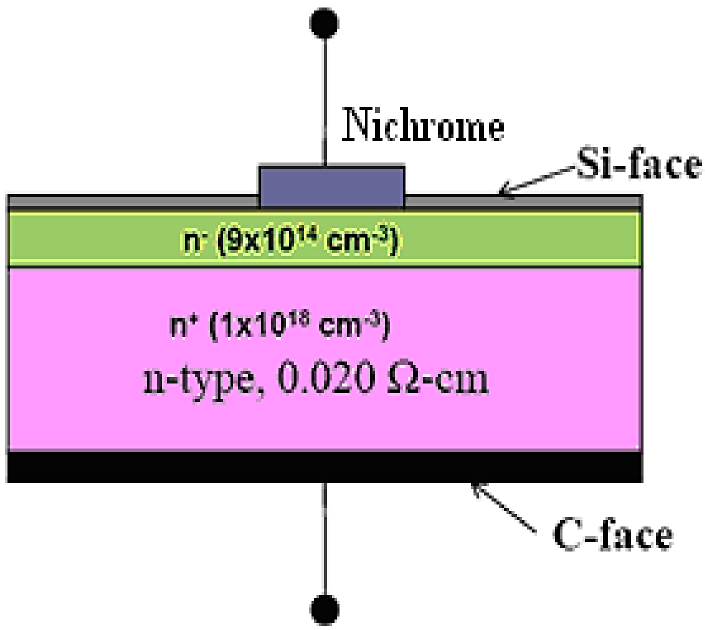

Figure 1. Schematic crossectional diagram of Schottky barrier diode.

3. RESULTS AND DISCUSSION

According to thermionic-emission theory, the current-voltage (I-V) relationship for Schottky diode can be expressed as [20]

$$J = J_s[\exp(\frac{qV}{kT}) - 1] \quad (1)$$

where: $J_s = A^* T^2 \exp(\frac{-q\phi_B}{kT})$

represents the reverse saturation current density, q is the electronic charge, A^* is the Richardson's constant (146 A/cm^2K^2) for 4H-SiC [21], ϕ_B is the barrier height, k is the Boltzmann constant, T is temperature in K and V is the forward volte. However the measured devices were found to follow the I-V relationship given in equ. (2).

$$J = J_s[\exp(\frac{qV}{nkT}) - 1] \quad (2)$$

If the applied voltage V is larger than 3 kT/q, exponential term in equ. (1) dominates and J can be approximated as:

$$J = J_s \exp(\frac{qV}{nkT}) \tag{3}$$

where: n is ideality factor and, n = 1 for thermionic emission theory.

Fig. (2) shows the forward I-V characteristics of a typical device for as deposited as well as devices annealed at four different temperatures. The ideality factor calculated from the slope of the linear region of the forward bias J-V characteristics using the relation:

$$n = \frac{q}{kT}\frac{dV}{d(\ln J)} \tag{4}$$

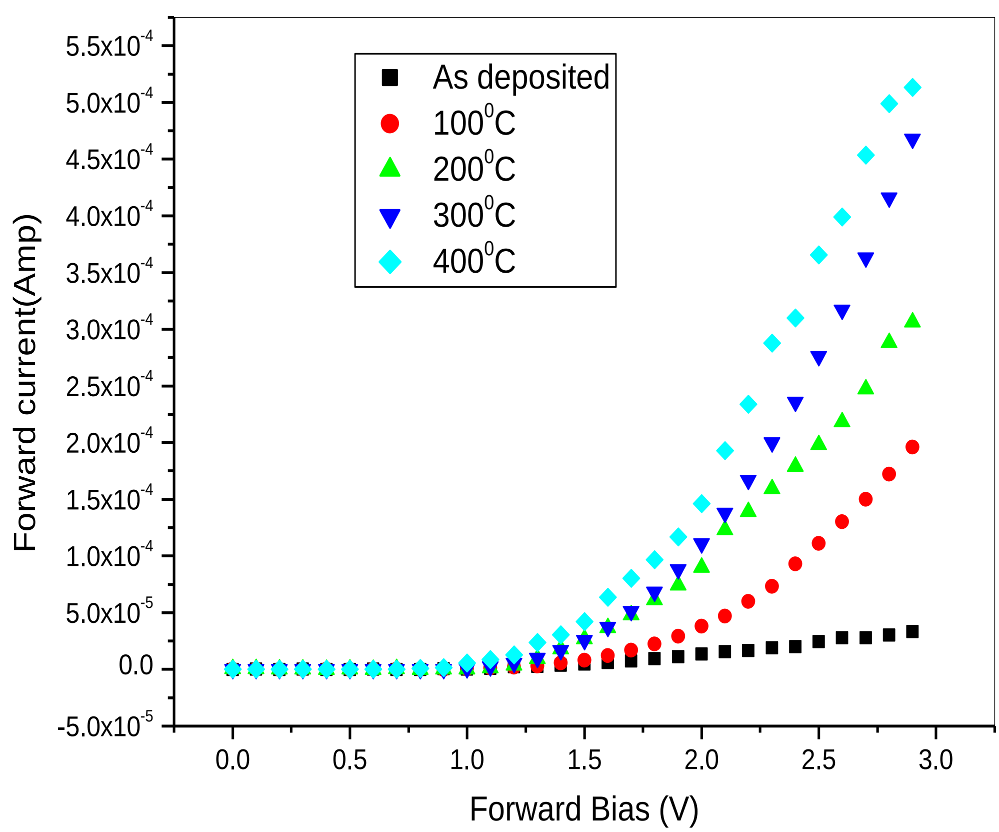

Figure 2. Forward I-V characteristics of Nichrome/4H-SiC Schottky diodes at deposited temperature and after annealing process.

The extrapolated value of the current density to zero voltage was used to obtain the reverse saturation current density J_s. The barrier height was obtained from the relation

$$\phi_B = \frac{kT}{q}\ln(\frac{A^*T^2}{J_s}) \qquad (5)$$

A barrier height of 0.79 eV and an ideality factor of 1.96 were calculated for the as-deposited Nichrome/4H-SiCSBDs. For an ideal Schottky diode the current flows due to the thermionic emission and the barrier height is independent of the bias voltage and the ideality factor is unity. Higher values of n can be attributed to the presence of thin oxide interfacial layer, the bias dependence of the barrier height due to image force barrier lowering, electron tunnelling through the potential barrier and the diode series resistance.

The I-V measurement is the most commonly used techniques for determining the transport mechanism in Schottky diodes. In order to get a clear understanding of the transport mechanism through Nichrome/4H-SiCsystem I-V characteristics were measured at room temperature after every thermal anneal in the temperature range from 25-400 ºC. In this work RTA was performed upto 400 ºC for 20 min in nitrogen ambient. I-V barrier height and ideality factor for Nichrome/4H-SiCSchottky diodes for as deposited as well as after each RTA process step are tabulated in Table (1). These values show an improvement in barrier height and ideality factor after RTA.

Table 1. Nichrome/4H-SiCSchottky diodes Electrical parameters deduced from I-V and C-V characteristics after RTA at different temperatures.

Annealing Temperature (ºC)	IV barrier height (eV)	CV barrier height (eV)	Ideality Factor
As-deposited	0.79	1.53	1.96
100	0.90	1.54	1.75
200	0.97	1.39	1.43
300	1.02	1.22	1.20
400	1.13	1.27	1.12

Fig. 3. shows current density-voltage (J-V) plots of typical Nichrome/4H-SiC Schottky diode for as-deposited and thermally annealed up to 400 ºC. It has been observed that plots are linear for narrow range of current values at low temperature and the maximum linear behaviour is shown for plot at 300 ºC. Since there was deviation in linearity for the plot at 400 ºC in comparison to 300 ºC, so RTA was performed up to 400 ºC only.

Figure.4. shows the variation in barrier height and ideality factor of Nichrome/4H-SiC Schottky diode as a function of annealing temperature. It is seen that the barrier height increases and ideality factor decreases with an increase in annealing temperature [25-27].We believe that increase in barrier height from 0.79 eV for as-deposited to 1.13 eV for high temperature annealed diode is due to the metallurgical reactions taking place at the interface which probably reduces the interfacial oxide layer and causes the increase in the Schottky barrier height.

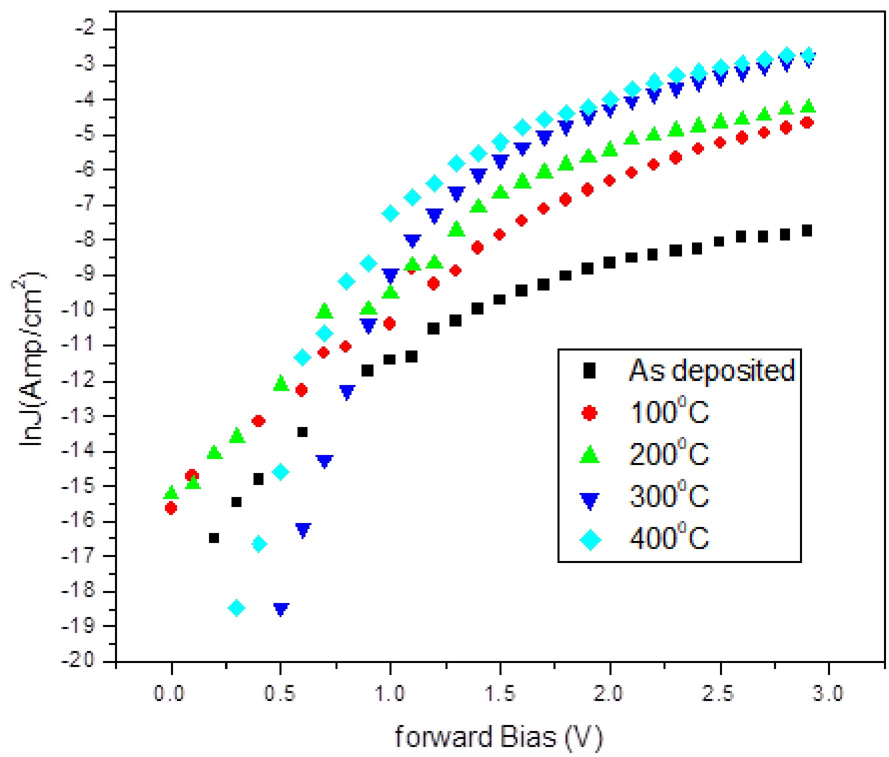

Figure 3. J-V characteristics of Nichrome Schottky diodes after different annealing temperature.

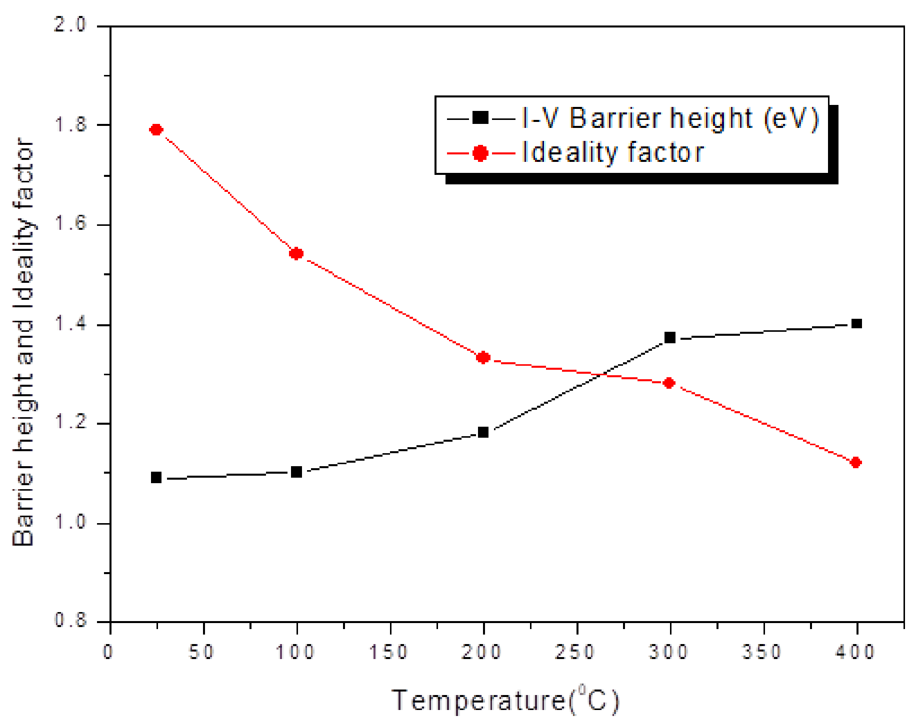

Figure 4. Dependence of I-V Barrier height and Ideality factor on Temperature.

Capacitance-voltage (C-V) measurements were also used for the extraction of SBH and doping concentration. When a small a.c. signal is superimposed upon a d.c. bias, charges of one type are induced on metal surface and charges of opposite type on the semiconductor. The depletion region capacitance per unit area can be expressed as

$$C = \sqrt{\frac{q\varepsilon_0\varepsilon_s N_D}{2[V_{bi} - V_R - (kT/q)]}} \tag{6}$$

where: N_D is the donor concentration; q, is the electronic charge; k, the Boltzman's constant; ε_s, is the permittivity of the semiconductor: V_{bi}, the built in voltage; and V_R the applied voltage.

The slope of the $1/C^2$ vs. V plot is given by

$$\frac{d(1/C^2)}{dV_R} = \frac{-2}{A^2 N_D \varepsilon_s \varepsilon_0} \tag{7}$$

The donor concentration can be calculated from the measured slope and the barrier height from the intercept on the voltage axis [23]. Thus we obtain

$$\phi_B = V_i + V_n + \frac{kT}{q} - \Delta\phi \tag{8}$$

where: V_i represents the intercept on the voltage axis; $\Delta\phi$, the image force barrier lowering; and V_n is the depth of the Fermi level below the conduction band. Plots of capacitance versus reverse bias generally gave good straight lines and a typical plot for as-deposited diode is shown in Fig. (5). Similar plots were obtained for thermally annealed diodes. From the slope of these curves donor concentration N_D was calculated to be equal to 1.45×10^{15} cm^{-3} which is in good agreement with 9×10^{14} cm^{-1}, the value provided by the manufacturer. The barrier height values obtained from C-V measurements are tabulated in the Table 1. The image force barrier lowering $\Delta\phi$ has been ignored while calculating the barrier height. Barrier heights obtained from C-V measurements vary in the range from 1.53 to 1.27 eV. It is also observed that the barrier heights obtained from C-V measurements are significantly higher than those obtained from the forward I-V measurements and this difference can not be attributed to some experimental error. Similar observations have also been reported by other investigators [12]. A suggestion has been made [24] that while calculating the barrier height from the I-V method the ideality factor should also be included in the expression of the barrier height which means that in equation (1), J_s should be written as

$$J_s = A^* T^2 \exp\left(\frac{-q\phi_B}{nkT}\right) \tag{9}$$

$$\text{Or } \phi_B = n\frac{kT}{q}\ln\left(\frac{A^* T^2}{J_s}\right) \tag{10}$$

The reason behind this suggestion is that, the factors which are responsible for the deviation in the value of ideality factor from unity at higher bias voltage are also present at zero bias voltage. In particular not only interfacial layer affect the deviation in the ideality factor but also image force and surface charges which will be present at zero bias. So mere reduction of the applied voltage to zero does not result in the elimination of these effects. Barrier heights modified using this relation is shown in Table (2) where these are compared with the results of the C-V measurements. It is seen that new values of barrier height are in good agreement with those obtained from the C-V measurements.

Table 2. Barrier height deduced from I-V and C-V characteristics after RTA for Nichrome/4H-SiC Schottky diodes.

Annealing Temperature (ºC)	IV barrier height (eV)	New IV barrier height (eV)	CV barrier height (eV)
As-deposited	0.79	1.54	1.53
100	0.90	1.57	1.54
200	0.97	1.38	1.39
300	1.02	1.22	1.22
400	1.13	1.26	1.27

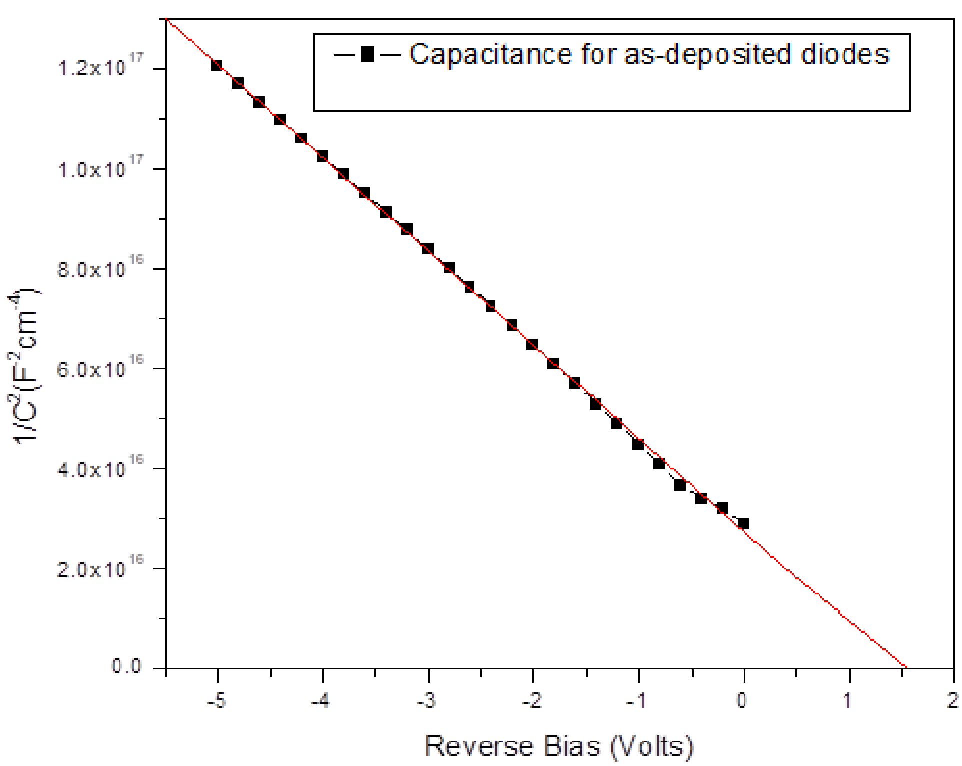

Figure 5. $1/C^2$ vs. voltage plot of the Nichrome/4H-SiC diode.

4. CONCLUSIONS

Electrical characteristics of Nichrome/4H-SiCSchottky contacts with thermal anneal from 25-400 ºC have been reported in this paper. The diodes were characterized using I-V and C-V measurement to extract parameters like barrier height, ideality factor and the doping concentration of the epilayer. Barrier heights calculated on as-deposited contacts were 0.79 eV and 1.53 eV from I-V and C-V techniques respectively. Diodes showed non-ideal behaviour at room temperature having ideality factor of 1.96 which improves to 1.12 after annealing at 400 ºC. It is concluded that, in this work, a better result has been possible simply by including the temperature dependant values of ideality factor in the expression of barrier height and this is demonstrated by comparing the new values of the barrier height with the values obtained from the capacitance measurements. Rapid Thermal annealing was found to be an essential step to reduce the non-ideal nature of the diode. Measurements above 400 ºC could not be undertaken.

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