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Finite control set MPC of LCL-filtered grid-connected power converter operating under grid distortions

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Abstract. Most of the basic control methods of the grid-connected converter (GCC) are defined to work with a sine wave grid voltage. In that case if the grid voltage is distorted by higher harmonics, the grid current may be distorted too, which, in consequence, may increase the value of the THD of the grid voltage. The paper deals with an improved finite control set model predictive control (FCS-MPC) method of an LCL-filtered GCC operating under distorted grid conditions. The proposed method utilizes supplementary grid current feedback to calculate the reference converter current. The introduced signal allows to effectively improve the operation when the grid is subject to harmonic distortion. The paper shows a simulation analysis of the proposed control scheme operating with and without additional feedback under grid distortions. To validate the practical feasibility of the proposed method an algorithm was implemented on a 32-bit microcontroller STM32F7 with a floating point unit to control a 10 kW GCC. The laboratory test setup provided experimental results showing properties of the introduced control scheme.

Key words: finite control set model predictive control FCS-MPC, grid-connected converters (GCCs), inductive-capacitive-inductive (LCL) filter, unbalanced grid, higher harmonics.

1. Introduction

Three phase grid-connected converters (GCC) are increasingly used in electric power systems due to their advantages such as power regeneration, adjustable power factor, control of the DC-link voltage and a low THD factor of the grid current [1, 2].

In most cases GCCs are L-, LC- or LCL-filtered. As LCL is a third-order low pass filter, it has better switching ripple attenuation with lower inductance compared with L and LC filters [3]. Nevertheless, to make use of the mentioned advantage the control scheme should consider the resonance frequency of an LCL filter [4]. Without proper damping, the resonance frequency leads to the increase of the grid current THD factor. The next problem faced by the control algorithm of a GCC with an LCL filter is work under grid disturbances such as higher harmonics grid voltage unbalance and dips. Because a GCC with an LCL filter is a more complicated system, supply voltage harmonics are the cause of a lower quality of the grid current in comparison to an L filter [5, 6]. Also, the grid voltage unbalance causes the appearance of low-order harmonics in the input current [7].

The problem of occurrence of LCL filter resonance frequency can be solved using passive or active damping methods [8]. Generally, active damping methods are more preferable because of lower power losses despite the increase in the complexity of the control algorithm. In [9] lead-lag network method of active damping was introduced and further developed in [10]. A simple voltage sensorless active damping scheme which does not introduce any extra sensors was proposed in [11]. In [12] a digital biquad filter, which consists of a resonance and a notch, is proposed to damp the LCL resonance. The above control schemes have been developed for linear algorithms with a PWM modulator and they are not intended for nonlinear control such as finite control set model predictive control (FCS-MPC). In FCS-MPC methods, which are now one of the fastest developing control concepts, the resonance harmonics were damped using a virtual resistance [13], multivariable cost function [14–16] or in combination with proportional resonant current controller [17].

Due to the fact that most of the basic control methods of a GCC are defined to work with a sine wave grid voltage, the operation during disturbances of the grid voltage is currently under thorough investigation [18-20]. Voltage Oriented Control (VOC), which is the most established control scheme of GCCs, uses PI controllers in a synchronous rotating reference frame to control grid current vector components proportional to active and reactive power. However, PI controllers have limited robustness to harmonic distortion. In [18, 21] to overcome this disadvantage a selective multi-reference system was used for each harmonic to be eliminated. An alternative to the above solution is the use of the proportional-resonant (PR) controllers for selective harmonic compensation [22]. Virtual torque-based control was introduced to cope with grid imbalance and harmonics in paper [19]. The proposed method allowed to change from unbalanced grid current to symmetrical current when necessary. In the above referenced works [18–22], to improve the grid current quality, control schemes had to be expanded and

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made complicated in consequence. In this context the use of the FCS-MPC methods could be a good alternative for the linear algorithms.

In [23, 24] the authors have tested the performances of the FCS-MPC-controlled GCC operating as a shunt active power filter (SAPF) during highly distorted grid voltage. The achieved results present high immunity of the proposed algorithms to the grid voltage disturbances. Those methods provide proper current control under grid voltage disturbances, such as higher harmonics voltage dips and unbalance. However, those algorithms were designed for an L-filtered GCC and cannot be used with an LCL filter.

In [16] the authors proposed and compared FCS-MPC methods which control parallelly the grid current, the converter current and the capacitor voltage. Thanks to that they can operate under grid distortions; however, a two-step scheme gave the lowest THD of the grid current. The main drawback of a longer horizon is the increase of a computational burden which makes the implementation in mainstream digital signal processors infeasible. Due to this, in [25] the author proposed an improvement which increased the robustness to higher harmonics but did not test this solution during unbalanced voltage.

This paper proposes a single step multiple-objective FCS-MPC method using error from additional grid current feedback. The algorithm improves the robustness to higher harmonics and unbalanced grid voltage and only slightly increases the computational burden. Thus, the development and implementation of the proposed algorithm using a single chip floating-point industrial microcontroller STM32F7 is possible. Both simulation and experimental results are presented to verify the effectiveness of the proposed control strategy.

2. The control system

The general structure of the two-level GCC connected to the grid through an LCL filter that is implemented in this work was shown in Fig. 1. The system is modelled in the dq rotating reference frame that rotates synchronously with the grid voltage vector.

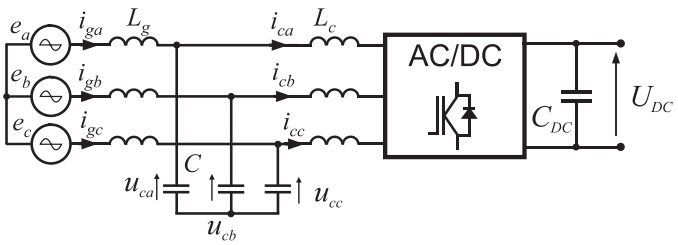

Fig. 1. Three-phase GCC connected to the grid through an LCL filter

By omitting parasitic resistances, the dynamic model of the GCC with an LCL filter can be expressed as follows:

$$L_g \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{gdq} = \boldsymbol{e}_{dq} - j\omega_g L_g \boldsymbol{i}_{gdq} - \boldsymbol{u}_{cdq}\,, \tag{1}$$

$$L_c \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{cdq} = \boldsymbol{u}_{cdq} - j\omega_g L_c \boldsymbol{i}_{cdq} - \boldsymbol{u}_{dq}\,, \tag{2}$$

$$C \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{u}_{cdq} = \boldsymbol{i}_{gdq} - \boldsymbol{i}_{cdq} - j\omega_g C \boldsymbol{u}_{cdq}\,, \tag{3}$$

where $\boldsymbol{i}_{gdq}$ is a grid-side current space-vector, $\boldsymbol{i}_{cdq}$ is a converter-side current space-vector, $\boldsymbol{e}_{dq}$ is a phase-to-neutral grid voltage space-vector, $\boldsymbol{u}_{cdq}$ is a filter capacitance C voltage space-vector, $\boldsymbol{u}_{dq}$ is a converter output voltage space-vector, L_g, L_c, and C are the values of the reactive elements of the LCL filter, ω_g is a grid angular frequency. The converter voltage vector $\boldsymbol{u}_{dq}$ can be described as follows:

$$\boldsymbol{u}_{dq} = \begin{cases} \dfrac{2}{3} U_{DC} e^{j\left[(n-1)\frac{\pi}{3} - \omega_g t\right]} & \text{for } n = \{1, 2, 3, 4, 5, 6\}, \\ 0 & \text{for } n = \{0,\ 7\}. \end{cases} \tag{4}$$

In [16], the authors proposed multivariable FCS-MPC methods to control an LCL-filtered GCC. The idea of the proposed methods lies in computing the references for the capacitor voltage and the converter-side current basing on the reference grid-side current. This facilitates including the whole state of the system in the cost function instead of using only the system output, i.e. grid-side current. In summary, the methods presented in [16] directly control three variables connected with an LCL filter, i.e. capacitor voltage $\boldsymbol{u}_{cdq}$, grid $\boldsymbol{i}_{gdq}$ and converter current $\boldsymbol{i}_{cdq}$. As a result, the resonance harmonics of an LCL filter were damped improving the quality of the grid current.

The grid voltage as a result of nonlinear loads, especially in the case of weak grid conditions, could be distorted by higher harmonics. Thus, the control algorithm should work well also under the distorted grid voltage condition. In [16] the presented control methods were examined for the case where the grid was subject to harmonic distortion. Two-step prediction achieved the lowest distortion of the grid current, but the computational burden was much higher than for the one-step counterpart. A longer horizon requires the use of more powerful (and therefore more expensive) DSPs or FPGAs, which may be not acceptable for industrial purposes.

In the following part of this paper the analysis of one-step method (in [16, 25]) during work with voltage harmonic distortions will be presented. As it is known in the dq rotating reference frame, the desirable grid current has a constant value which corresponds to a sinusoidal grid current in the natural reference frame (see Figs. 2a and 2b). If in the grid the current is distorted from the sine wave, then in the synchronous reference frame we can observe harmonic pulsation of the DC values of d and q components (see Figs. 2c and 2d). As a consequence, the grid current has a different value than the reference.

This knowledge was used in the proposed improved one-step multivariable FCS-MPC which works based on the scheme depicted in Fig. 3 and was implemented in the following steps.

Step 1. The measurement of the controlled variables of currents and voltages, synchronization with the grid (DSOGI-PLL), coordinate transformations.

Step 2. The computing of reference variables. The reference grid current component i_{gd}^* is a product of a DC-link voltage

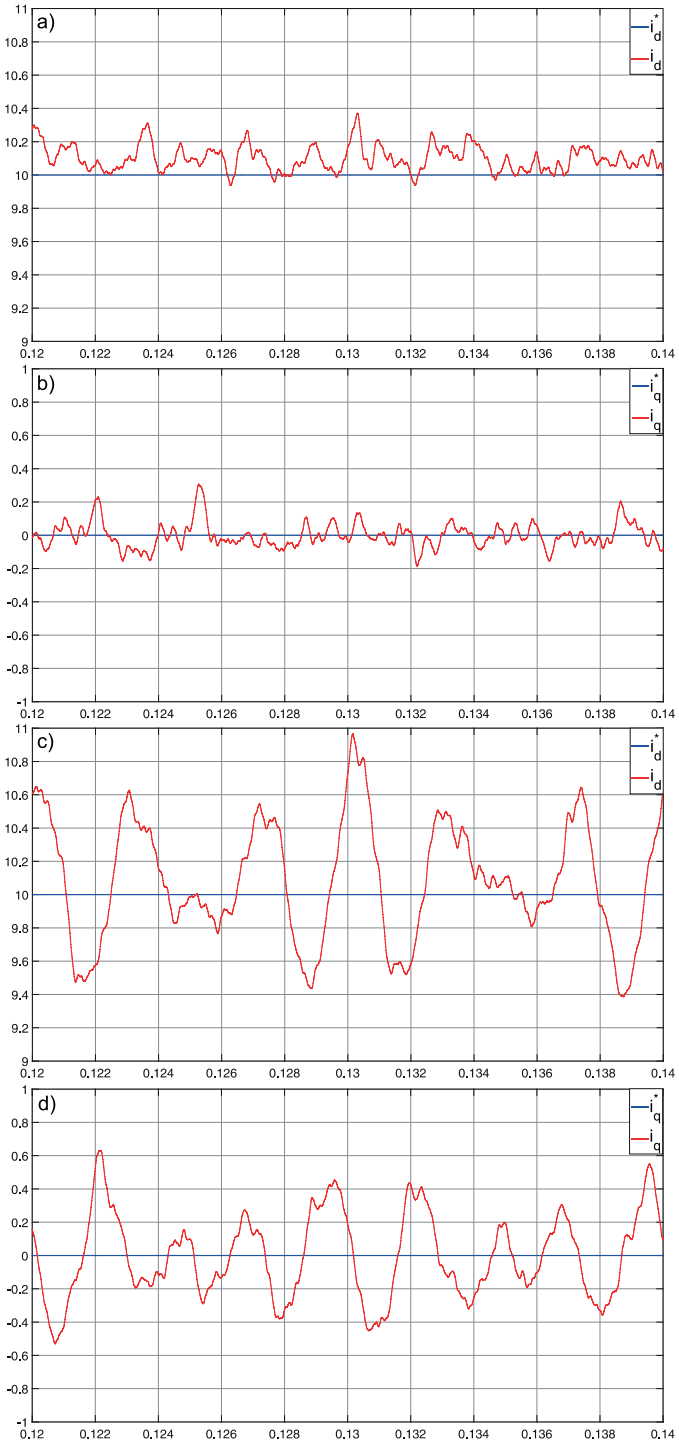

Fig. 2. Grid current vector components $\boldsymbol{i}_{gd}$ and $\boldsymbol{i}_{gq}$ under sinusoidal grid voltage conditions (a), (b) and under harmonic distortions (c), (d)

controller (proportional to active power P), $i^*_{gq}$is proportional to reactive power Q. Using the reference grid current vector $\boldsymbol{i}^*_{gdq}$, the reference capacitance voltage vector is calculated (5):

$$\boldsymbol{u}^*_{cdq} = \boldsymbol{e}_{dq} - j\omega_g L_g \boldsymbol{i}^*_{gdq}\,. \tag{5}$$

The idea of the proposed control scheme is to calculate the error between the reference and measured grid current components in

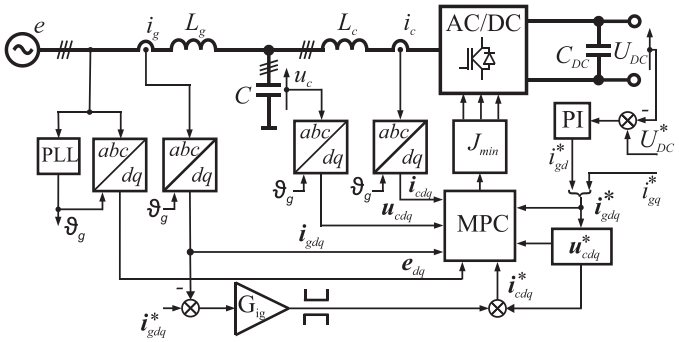

Fig. 3. Schematic diagram of the proposed control method

the dq reference frame. Next, the error is multiplied by the gain G_{ig} and added to the reference value of the converter current vector:

$$\boldsymbol{i}^*_{cdq} = \boldsymbol{i}^*_{gdq} - j\omega_g C \boldsymbol{u}^*_{cdq} + \left(\boldsymbol{i}^*_{gdq} - \boldsymbol{i}_{gdq}\right) G_{ig}\,. \tag{6}$$

The proposed algorithm uses an assumption that for short enough sampling time T_s the reference values from step (k) do not change in step $(k{+}1)$:

$$\boldsymbol{i}^*_{gdq}(k+1) \approx \boldsymbol{i}^*_{gdq}(k), \tag{7}$$

$$\boldsymbol{u}^*_{cdq}(k+1) \approx \boldsymbol{u}^*_{cdq}(k), \tag{8}$$

$$\boldsymbol{i}^*_{cdq}(k+1) \approx \boldsymbol{i}^*_{cdq}(k). \tag{9}$$

Step 3. Computing the predictions of the three controlled variables in the next sampling step $(k{+}1)$ for all possible GCC output voltage vectors based on the discrete-time model of the LCL.

The predicted converter current vector $\boldsymbol{i}_{cdq}(k{+}1)$ can be expressed as:

$$\Delta\boldsymbol{i}_{cdq}(k+1) = \frac{\boldsymbol{u}_{cdq}(k) - j\omega_g L_c \boldsymbol{i}_{cdq}(k) - \boldsymbol{u}_{dq}(k+1)}{L_c} T_s\,, \tag{10}$$

$$\boldsymbol{i}_{cdq}(k+1) = \boldsymbol{i}_{cdq}(k) + \Delta\boldsymbol{i}_{cdq}(k+1). \tag{11}$$

The future capacitance voltage vector $\boldsymbol{u}_{cdq}(k+1)$ can be determined:

$$\Delta\boldsymbol{u}_{cdq}(k+1) = \\ = \frac{\boldsymbol{i}_{gdq}(k) - j\omega_g C \boldsymbol{u}_{cdq}(k) - \boldsymbol{i}_{cdq}(k) - 0.5\Delta\boldsymbol{i}_{cdq}(k+1)}{C} T_s\,, \tag{12}$$

$$\boldsymbol{u}_{cdq}(k+1) = \boldsymbol{u}_{cdq}(k) + \Delta\boldsymbol{u}_{cdq}(k+1). \tag{13}$$

The predicted grid current vector $\boldsymbol{i}_{gdq}(k+1)$ is obtained using the equations:

$$\Delta\boldsymbol{i}_{gdq}(k+1) = \\ = \frac{\boldsymbol{e}_{dq}(k) - j\omega_g L_g \boldsymbol{i}_{gdq}(k) - \boldsymbol{u}_{cdq}(k) - 0.5\Delta\boldsymbol{u}_{cdq}(k+1)}{L_g} T_s\,, \tag{14}$$

$$\boldsymbol{i}_{gdq}(k+1) = \boldsymbol{i}_{gdq}(k) + \Delta\boldsymbol{i}_{gdq}(k+1). \tag{15}$$

The nature of the operation of the microprocessor control system causes a delay between the start of sampling and the selection of a new GCC output voltage vector (sending new switching state). This delay is caused by a specific conversion time of the analog to digital converter (ADC) and the calculation time, among other things. This issue was solved with a simple delay compensation scheme using the same equations but with the shift one step forward in time [26].

Step 4. The determination of the expected errors between the reference and the predicted values using the following equations:

$$\varepsilon_{icdq}(k+1) = \boldsymbol{i}^*_{cdq}(k+1) - \boldsymbol{i}_{cdq}(k+1), \tag{16}$$

$$\varepsilon_{ucdq}(k+1) = \boldsymbol{u}^*_{cdq}(k+1) - \boldsymbol{u}_{cdq}(k+1), \tag{17}$$

$$\varepsilon_{igdq}(k+1) = \boldsymbol{i}^*_{gdq}(k+1) - \boldsymbol{i}_{gdq}(k+1). \tag{18}$$

Step 5. The selection of the optimal GCC voltage vector which will be used in step (k), based on the minimum value of the following cost function:

$$\begin{aligned} J = {} & w_{ig}^2 \left(\varepsilon_{igd}^2(k+1) + \varepsilon_{igq}^2(k+1)\right) + \\ & + w_{uc}^2 \left(\varepsilon_{ucd}^2(k+1) + \varepsilon_{ucq}^2(k+1)\right) + \\ & + \left(\varepsilon_{icd}^2(k+1) + \varepsilon_{icq}^2(k+1)\right) + w_{fsw} n_{sw}\,. \end{aligned} \tag{19}$$

The n_{sw} component included in the cost function (20) is responsible for the average switching frequency f_{sw} reduction. The predicted number of switching is obtained as follows:

$$\begin{aligned} n_{sw} = {} & |S_a(k+1) - S_a(k)| + |S_b(k+1) - S_b(k)| + \\ & + |S_c(k+1) - S_c(k)|\,, \end{aligned} \tag{20}$$

where $S_x(k+1)$ is the predicted switching state for the next sampling period $(k+1)$. $S_x(k)$ is the currently used switching state.

3. Simulations study

The proposed control method was implemented and examined in simulation studies. The simulation model was built in Matlab Simulink package. The presented results have been performed with the sampling time $T_s = 20$ µs and the rated power $P =$ 5.0 kW. The parameters of the system are presented in Table 1. To synchronize the system with the grid voltage Dual Second Order Generalized Integrator (DSOGI-PLL) was used [27].

In Fig. 4 the waveforms of grid phase current i_{ga} and grid voltage e_a under sinusoidal grid conditions are shown for gain $G_{ig} = 0$. It can be seen that if the grid voltage is sinusoidal the THD of the grid current is 1.1%.

The results presented next concern an operation under the distorted voltage condition in which the grid voltage THD = 6.1% (distorted by 4.3% of the 5th and 7th harmonics). In this situation the THD of the grid current is 3.5% for the gain Gig = 0 (see Fig. 5). Fig. 6 depicts operation results for the

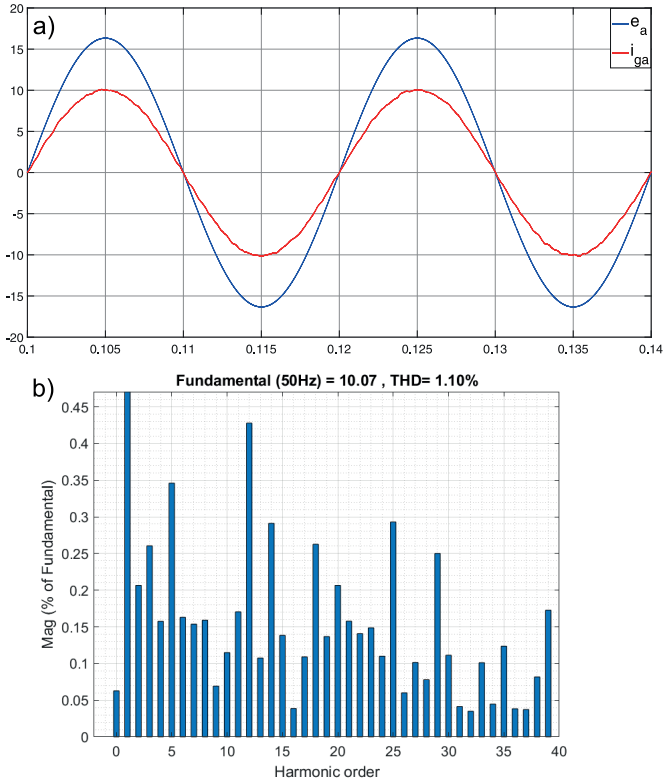

Fig. 4. a) Grid phase voltage e_a (100 V/div) and current i_{ga} (5 A/div), b) THD of the grid current during sinusoidal grid voltage condition where the gain $G_{ig} = 0$

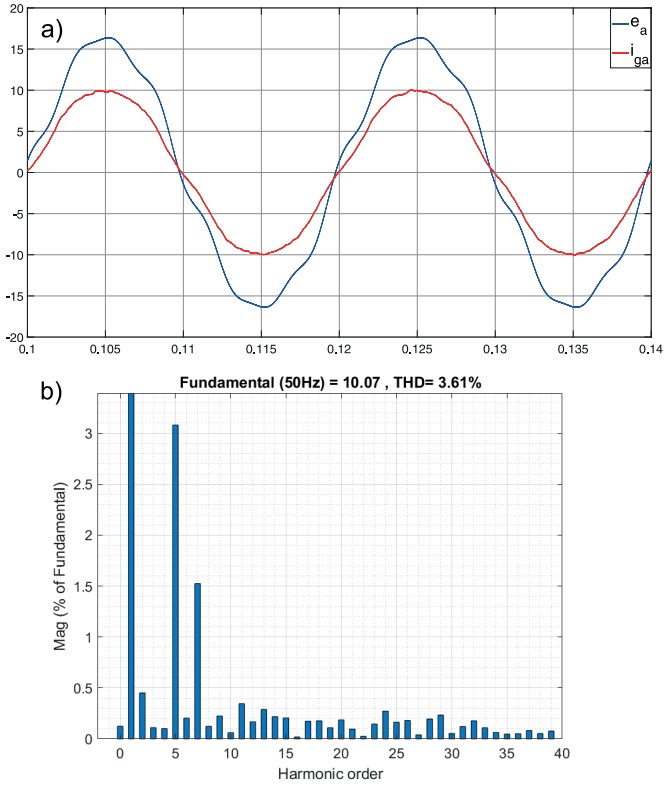

Fig. 5. a) Grid phase voltage e_a (100 V/div) and current i_{ga} (5 A/div), b) THD of the grid current during distorted grid voltage condition where the gain $G_{ig} = 0$

gain Gig = 4. The value of the grid current THD was reduced to 1.5%, which proves the effectiveness of the proposed control method. Fig. 7 shows that, compared to Figs. 2c and 2d, the oscillations of the grid current vector components were definitely reduced.

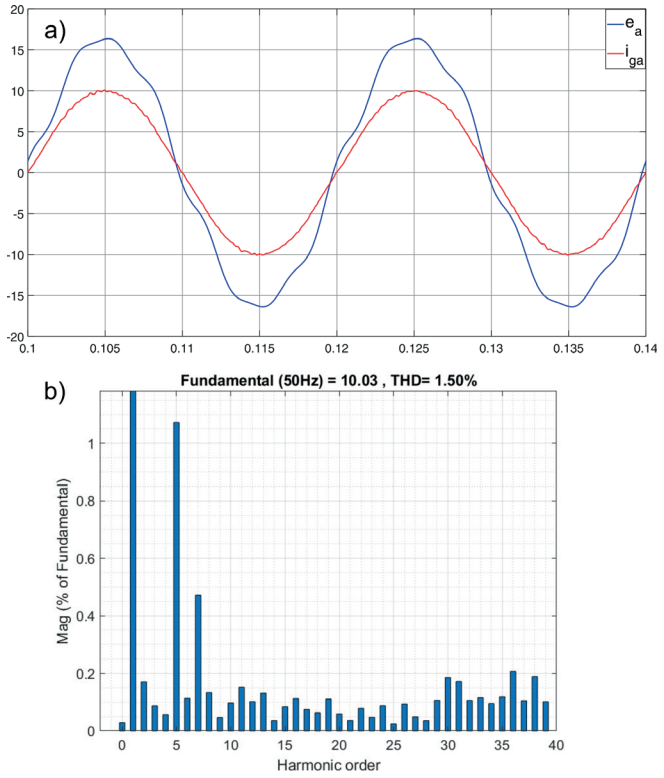

Fig. 6. a) Grid phase voltage e_a (100 V/div) and current i_{ga} (5 A/div), b) THD of the grid current during distorted grid voltage condition where the gain $G_{ig} = 4$

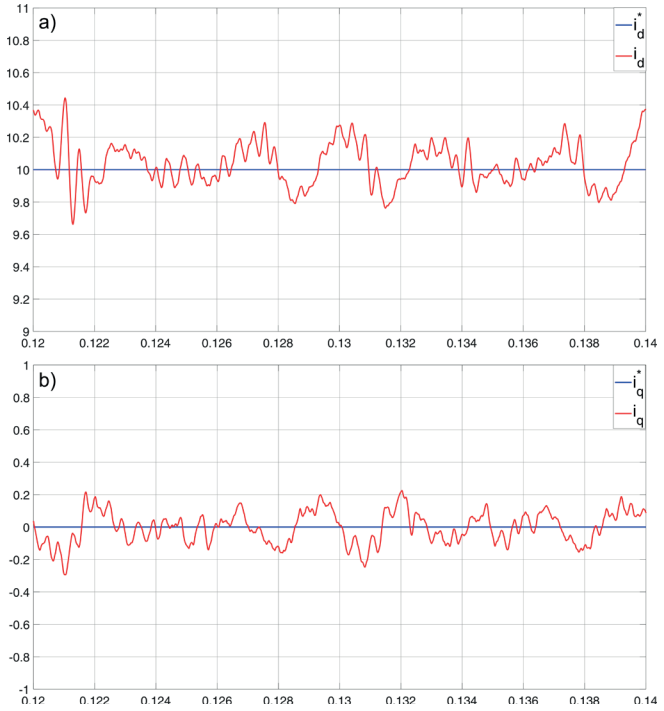

Fig. 7. Grid current vector components i_{gd} and i_{gq} under harmonic distortions where the gain $G_{ig} = 4$

Table 1
System parameters

Variable	Parameters	Value
E	Grid-voltage	325 V
U_{DC}	DC capacitor voltage	650 V
$T_s(f_s)$	Sampling time (sampling frequency)	20 µs (50 kHz)
L_g	Grid-side inductor	1.8 mH
L_c	Converter-side inductor	3.4 mH
C	Filter capacitor	20 µF
f_r	L_g–C–L_c filter resonance frequency	1037 Hz

4. Experimental study

The proposed multivariable FCS-MPC algorithm with additional grid current feedback was verified experimentally in a two-level GCC with an LCL filter connected to a three-phase grid. The parameters of the setup were listed in Table 1. The programmable AC source (California Instruments MX30-3Pi) was utilized to generate grid voltage disturbances. The use of a power analyzer Yokogawa WT 1800 allowed us to measure the THD factors and present the recorded waveforms. The control algorithm was implemented using a low-cost floating-point digital signal microcontroller STM32F7 operating at 216 MHz. The computational delay associated with the FCS-MPC was compensated using the method proposed in [26]. The converter operated with the unity power factor $Q = 0$ kvar ($i^*_{gq} = 0$ A) and the active power $P = 5$ kW.

Fig. 8 presents the experiment results under sinusoidal grid voltage in a steady state where the THD of the grid current is

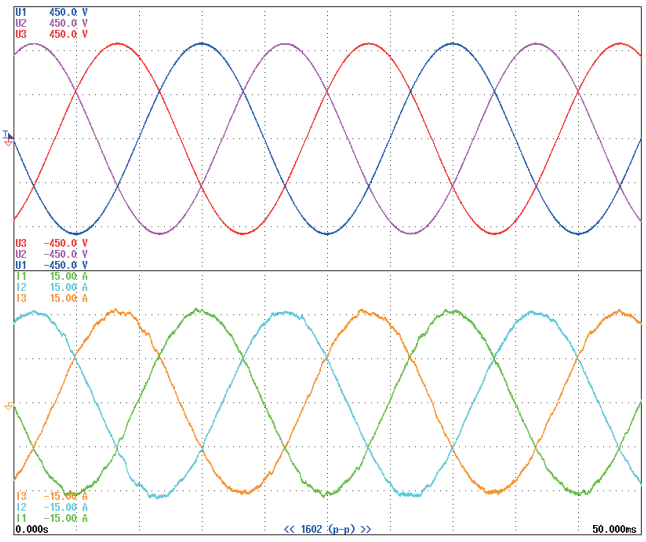

Fig. 8. The grid phase voltages (150 V/div) and currents (5 A/div) under sinusoidal grid voltage where the gain $G_{ig} = 0$

1.9% for the gain $G_{ig} = 0$. To show the contribution of the additional grid current feedback, first the results for the gain $G_{ig} = 0$ under distorted voltage conditions were presented in Fig. 9a.

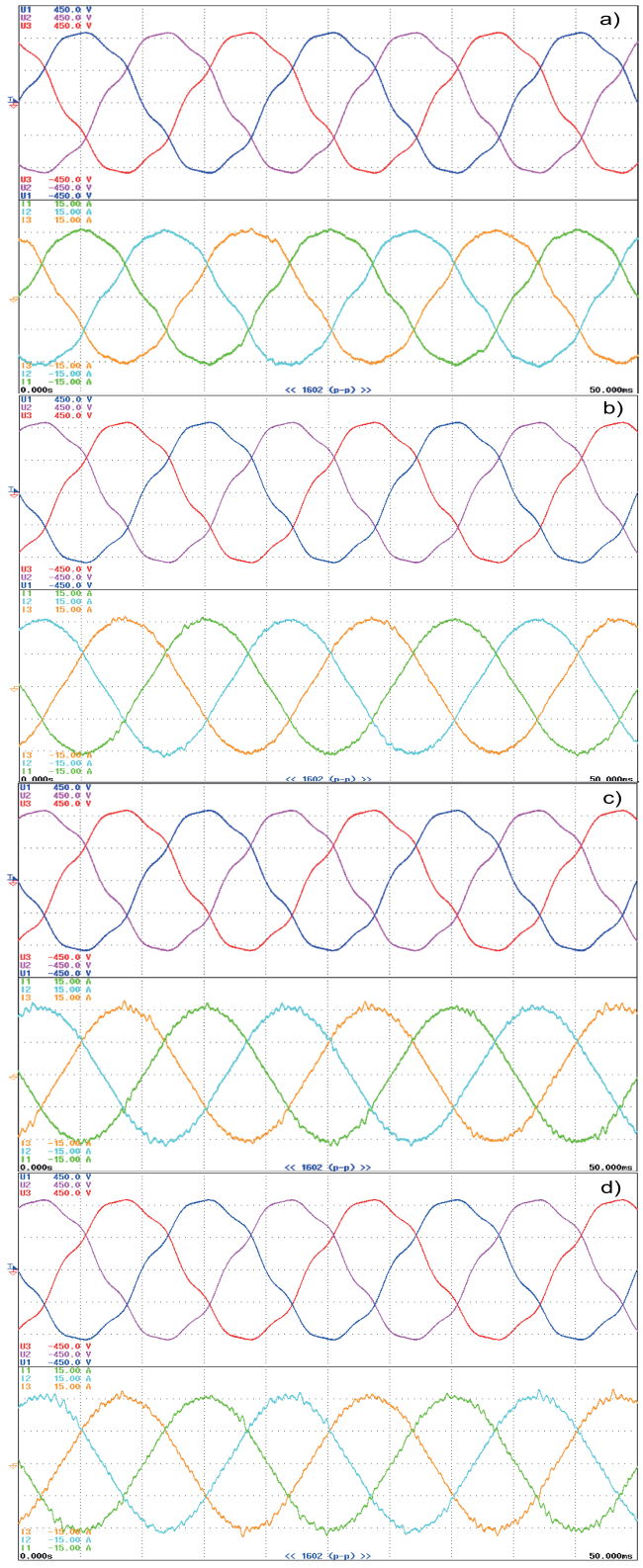

Fig. 9. The grid phase voltages (150 V/div) and currents (5 A/div) under sinusoidal grid voltage where the gain (a) $G_{ig} = 0$, (b) $G_{ig} = 4$, (c) $G_{ig} = 10$, (d) $G_{ig} = 60$

The grid voltage was distorted by 4.3% of the 5th and 7th harmonics and THD was 6.1%. In this case the THD of the grid current increased to 4.0%. Next, the waveforms of grid voltages and currents (see Figs. 9b, 9c and 9d) were recorded for the gain $G_{ig} = 4$, 10 and 60, respectively, and the values of THD and the average switching frequency $f_{sw(av)}$ were compared in Table 2. Additionally, the THD of the grid current was shown in Fig. 10 during the change of the gain G_{ig} from 0 to 60. The presented results demonstrate that the additional feedback improves the quality of the grid current in distorted voltage conditions. Fig. 10 shows that for the gain G_{ig} from 4 to 10 the THD of the grid current has the lowest values. Fig. 9d shows that the grid current for the $G_{ig} = 60$ has high frequency components but still the value of the THD is lower than for $G_{ig} = 0$. For further experimental tests $G_{ig} = 4$ was used.

Table 2
Comparison of the THD values of the grid current during change of the gain G_{ig} – experimental results

G_{ig}	THD of the grid current [%]	$f_{sw(av)}$ [kHz]
0	4.0	7.3
4	2.3	7.3
10	2.3	7.3
60	3.3	6.7

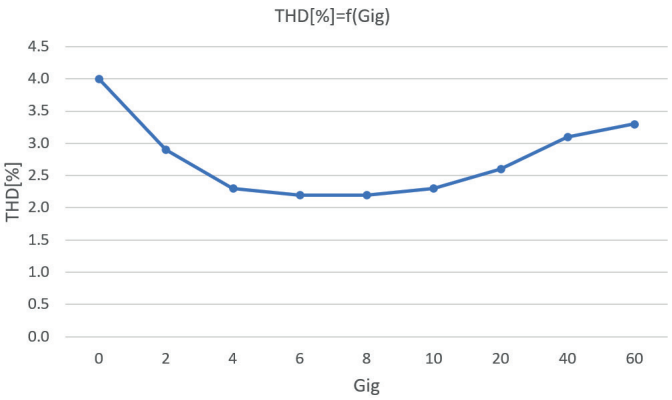

Fig. 10. Comparison of the THD values of the grid current during change of the gain G_{ig} from 0 to 60 – experimental results

In the next step the control scheme was tested during grid voltage unbalance ($e_a = 50\%$ of the nominal value). In this case Fig. 11 depicts a symmetrical grid current and THD equal to 1.1%. Another case, in which the grid voltage was at the same time unbalanced and distorted (in single phase), was tested. This instance (see Fig. 12) presents the capability of the proposed control algorithm to provide symmetrical grid currents with a low content of higher harmonic under conditions of voltage distortion and unbalance.

In the last stage of experimental verification, the step response of the reference grid current was studied. During the

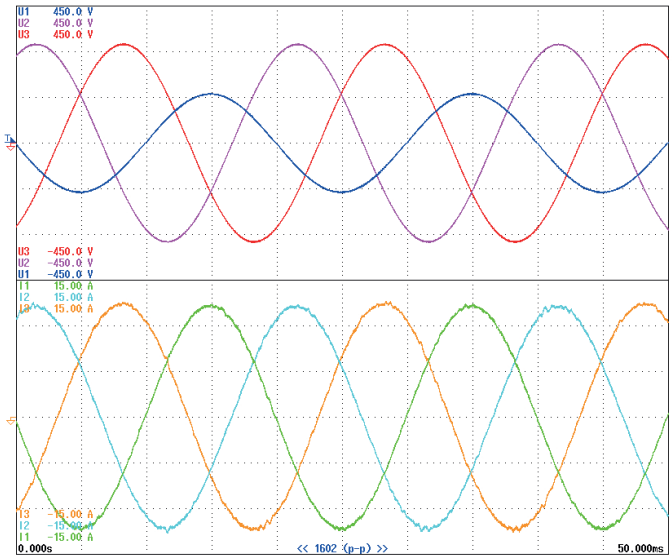

Fig. 11. The grid phase voltages (150 V/div) and currents (5 A/div) under grid voltage asymmetry for $G_{ig} = 4$

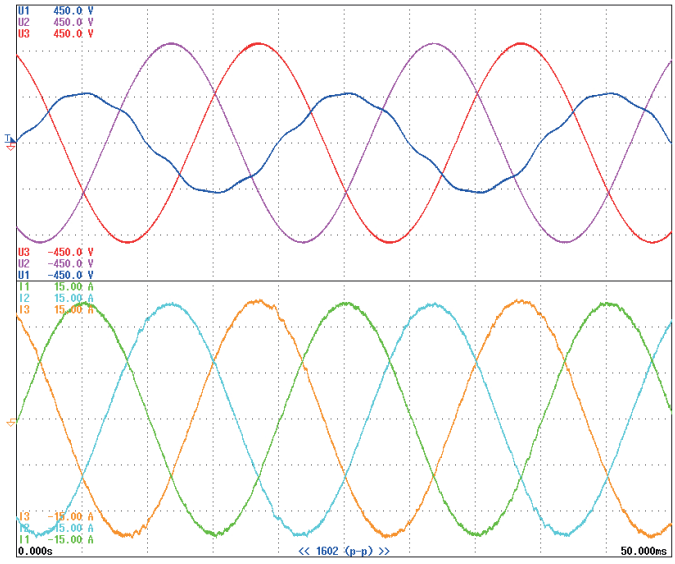

Fig. 12. The grid phase voltages (150 V/div) and currents (5 A/div) under grid voltage asymmetry and distortion for $G_{ig} = 4$

test, the setup worked under grid conditions shown in Fig. 12. The DC voltage regulator was turned off to eliminate its influence on the control system. Four reference grid current values were used:

$$i^*_{gd} = 3.7 \text{ A } (P = 1.8 \text{ kW}),$$

$$i^*_{gd} = 7.2 \text{ A } (P = 3.5 \text{ kW}),$$

$$i^*_{gd} = -2.1 \text{ A } (P = -1.0 \text{ kW}),$$

$$i^*_{gd} = 0 \text{ A } (P = 0 \text{ kW}).$$

The outcomes confirm stability in transient and static states, including transferring energy to the grid.

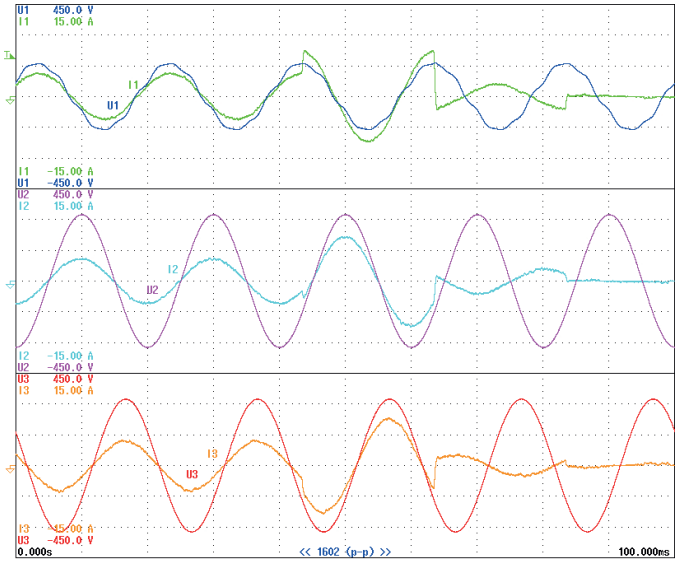

Fig. 13. The grid phase voltages (150 V/div) and currents (5 A/div) under grid voltage asymmetry and distortion for $G_{ig} = 4$ during the transient step change of the reference grid current

5. Conclusions

In this paper a multivariable FCS-MPC algorithm with additional feedback from the grid current for a three phase GCC with an LCL filter was proposed. Additional feedback was introduced to improve the robustness of the distorted and unbalanced grid voltage. Simulation and experimental investigations proved that the presented control method reduces the value of the THD factor of the grid current for both voltage disturbances. Furthermore, the algorithm does not increase the value of the average switching frequency, so there is no negative influence on the efficiency of the converter. This solution is straightforward, does not boost the computational burden, and can be implemented on a single-chip low cost floating-point microcontroller STM32F7.

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