BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES
Vol. 52, No. 3, 2004

# Multiple-input floating-gate MOS transistor in analogue electronics circuit

L. TOPÓR-KAMIŃSKI[1]* and P. HOLAJN[2]**

[1] Institute of Measurements and Automatic Control in Electrical Engineering, Silesian University of Technology, 10 Akademicka St., 44–100 Gliwice, Poland

[2] Institute of Theoretical and Industrial Electrotechnics, Silesian University of Technology, 10 Akademicka St., 44–100 Gliwice, Poland

**Abstract.** Conceptions of analogue electronics circuit based on a multiple-input floating gate field-effect transistor MOS (MIFGMOS) have been presented. The simple add and differential voltage amplifiers with one and two MIFGMOS transistors and multiple-input operational amplifiers with their application have been proposed. One of them was used for the realisation of a controlled floating resistor. Results of circuit simulations in SPICE programme using the simple substitute macromodel of MIFGMOS transistor have been shown.

**Keywords:** floating-gate MOSFET, analogue amplifier, voltage controlled resistor, multiple-input operational amplifier.

## 1. Introduction

Floating gate field-effect transistors have been applied in a digital circuit until quite recently. At present appear the propositions of application of FGMOS transistors in analogue circuits [1–4] especially non-linear circuit's in the form of multiple-terminal electronic devices, called then multiple-terminal MOS transistor with floating-gate (MIFGMOS). They have the same basic properties as equivalent ordinary MOS transistors but widened by certain additional features. The most significant of them, there is the ability of summing gate controlling input signals as well as the possibility of reduction of threshold value voltage $U_{TH}$. In some technological solution, the value of charge collected in floating gate can be additionally controlled. These transistors can operate as normal MOS as saturated or non-saturated within the region of strong inversion or atypically within the region of weak inversion called sub-threshold region. That second operating region is utilised in electronic circuits with very low supply voltage, even below one-volt [5].

## 2. Properties of FGMOS transistor

Floating-gate MOS transistor is generated by forming an additional conductive layer, between control terminal G and channel DS isolated from the environment, called floating gate. For transistors equipped with larger quantity of control terminals $G_i$ than one (MIFGMOS), they are contacting with that gate through the capacities $C_i$ created between them. Floating gate is contacting with the channel CH through the capacity of oxide layer $C_{0X}$ and with source, drains and bulks through the capacities $C_{FS}$, $C_{FD}$ and $C_{FB}$. Values of those capacities depend on the area of input gates $G_i$, floating gate FG and channel as well as on thickness of oxide layer between then, that is to say, on the shape of structure of the whole MIFGMOS transistor made on semiconductor (Fig. 1a).

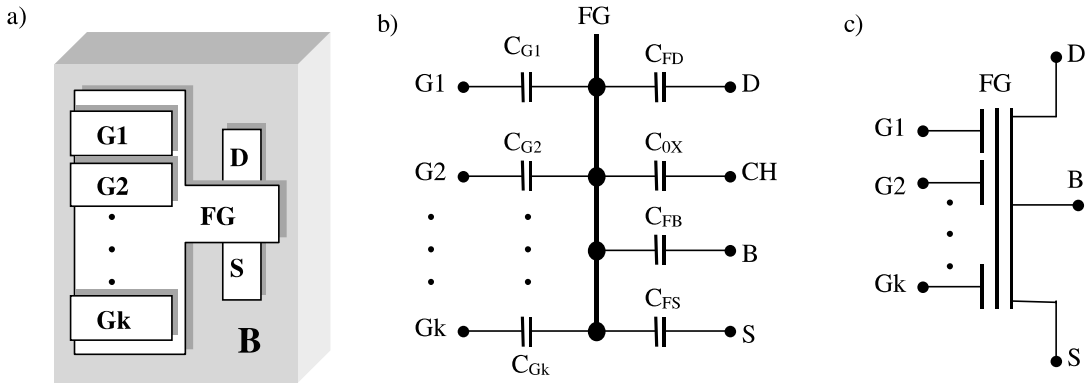


Fig. 1. Layout of $k$-input FGMOS (a), equivalent circuit model (b), and symbol (c)

* e-mail: ltk@polsl.gliwice.pl
** e-mail: piotr.holajn@polsl.pl

Potentials of transistor terminals $U_{Gi}$, $U_D$, $U_S$, $U_B$, floating gate potential $U_{FG}$ and charge $Q_{FG}$ collected on that gate as well as channel surface potential $\Psi_S$, exert the influence on the phenomenon's taking place in the channel and thus on drain current $I_D$. Depending on transistor design, operating conditions and values for individual potentials and capacities, one can state in many cases that floating gate potential is only a function of potential $U_{Gi}$ of input gate terminals summed with weights depending on $C_{Gi}$ and $C_T$ values, that means

$$U_{FG} = \sum_{i=1}^{k} w_i U_{Gi} \tag{1}$$

where:

$$w_i = \frac{C_{Gi}}{C_T} \tag{2}$$

where $C_T$ is the sum of all capacities connected with floating gate.

In the region of strong inversion and saturation of MIFGMS transistor with the channel of "n" type and under assumption that $U_B = 0$, drain current for that transistor is described by the following relation:

$$I_{DFG} = \beta \left( \sum_{i=1}^{k} w_i U_{Gi} - U_{TH} \right)^2 \tag{3}$$

in which $\beta = \mu C_{0X} W/L$ is a transconductance parameter and $U_{TH}$ — threshold voltage. Drain current for that transistor within non-saturated region has the following value:

$$I_{DFG} = \beta \left( \sum_{i=1}^{k} w_i U_{Gi} - U_S - U_{TH} \right) (U_D - U_S) - \frac{1}{2}(U_D - U_S)^2. \tag{4}$$

The most important properties of MIFGMOS transistor are the following: additional input control signals $U_{Gi}$ and possibility of threshold voltage $U_{TH}$ reduction. The circuits containing MIFGMOS transistors can be, basing on relation's (3) and (4) simulated using macromodel [3, 6] (Fig. 2) composed of MOS transistor as well as additional capacities of gates $C_{Gi}$ and controlled sources $w_i U_i$.

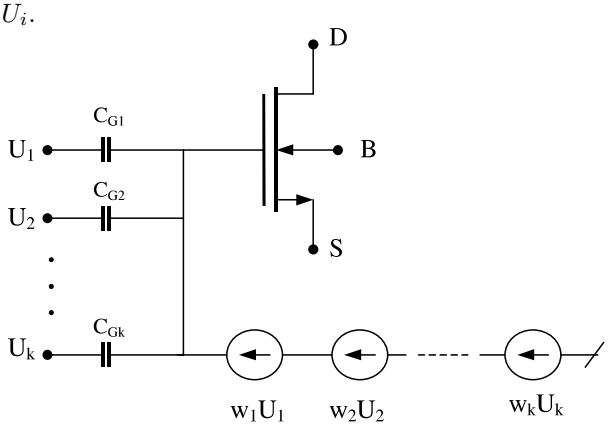


Fig. 2. Equivalent macromodel of $k$-input FGMOSFET

## 3. Simple voltage amplifiers with MIFGMOS transistor

Using MIFGMOS transistor with large number of input terminals $G_i$in above-mentioned amplifier, simple summing voltage amplifier as in Fig. 3 is obtained [4, 7].

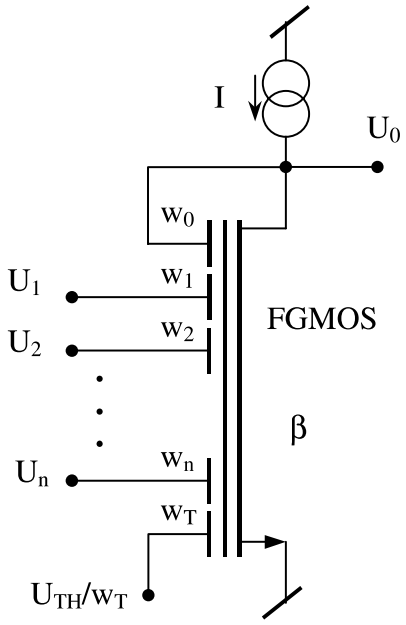


Fig. 3. Reversing/summing voltage amplifier with one MIFGMOS transistor

For operation within the saturation region that amplifier is described by the following dependence:

$$U_0 = \frac{1}{w_0}\sqrt{\frac{2I}{\beta}} - \sum_{j=1}^{n} \frac{w_j}{w_0} U_j = U_{00} - \sum_{j=1}^{n} k_j U_j. \tag{5}$$

And, at the same time following condition must be fulfilled:

$$\sum_{j=1}^{n} w_j U_j > (1 - w_0) U_0. \tag{6}$$

In order to obtain non-reversing voltage amplifier, two MIFGMOS transistors (in Fig. 4) should be applied. When the both transistors FGMOS1 and FGMOS2 will operate within the saturated region, the following equation will be obtained:

$$U_0 = \frac{\sqrt{2}}{w_{02}} \left( \sqrt{\frac{I_2}{\beta_2}} - \frac{w_2}{w_{01}} \sqrt{\frac{I_1}{\beta_1}} \right) + \frac{w_2}{w_{02}} \frac{w_1}{w_{01}} U_1 = U_{02} + k_{12} U_1. \tag{7}$$

It describes this circuit when input $U_1$ fulfils the following condition:

$$U_{1bounD} = \frac{w_{01}}{w_1} \left( \frac{1}{w_{01}} \sqrt{\frac{2I_1}{\beta_1}} - \frac{1 - w_{02}}{w_2} \sqrt{\frac{2I_2}{\beta_2}} \right) < U_1$$

$$< \frac{1-w_{01}}{w_1}\sqrt{\frac{2I_1}{\beta_1}} = U_{1bounG}. \tag{8}$$

where $U_{1bounD}$, $U_{1bounG}$ — boundary values.

If in the circuit (in figure 4) MIFGMOS transistors with next additional input terminals are applied summing/subtracting voltage amplifiers shown in Fig. 5, is obtained.

For the case when the both FGMOS1 and FGMOS2 transistors will operate within the saturated region, amplifier is described by the following equation:

$$U_0 = \frac{\sqrt{2}}{w_{02}}\left(\sqrt{\frac{I_2}{\beta_2}} - \frac{w_P}{w_{01}}\sqrt{\frac{I_1}{\beta_1}}\right) + \frac{w_P}{w_{01}}\frac{w_1}{w_{02}}U_1 + \\ + \frac{w_P}{w_{01}}\frac{w_2}{w_{02}}U_2 - \frac{w_3}{w_{02}}U_3 - \frac{w_4}{w_{02}}U_4. \tag{9}$$

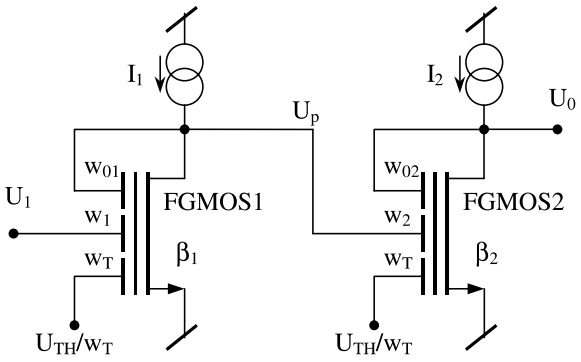


Fig. 4. Simple non-reversing voltage amplifier

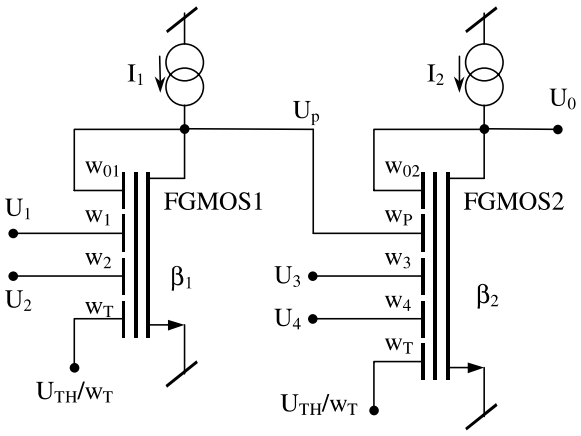


Fig. 5. Summing/subtracting voltage amplifier

## 4. Multiple-input OA with FGMOS transistors working in saturation region

Making connection of differential OA with the amplification A to the pair of FGMOS transistors (Fig. 3), working in the saturation region it was obtained multiple-input voltage OA circuit shown in Fig. 6.

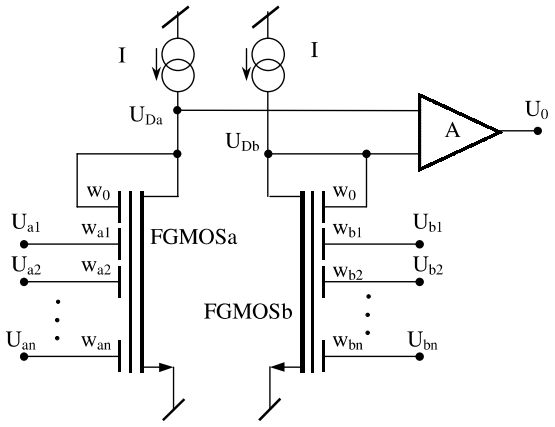


Fig. 6. Multiple-input OA with the pair of FGMOS transistorsg workin in the saturation region

Making an assumption that transistors are identical, have equal current supply and weight value, that is:

$$w_{a1} = ... = w_{an} = w_{b1} = ... = w_{b1} = w. \tag{10}$$

then it is described by relation:

$$U_0 = A\frac{w}{w_0}\left(\sum_{k=1}^{n} U_{ak} - \sum_{k=1}^{n} U_{bk}\right). \tag{11}$$

In order that transistors work in the saturation region each of them must fulfil the inequality:

$$\sum U_k \leqslant (1-w_0)\frac{w_0}{w}\sqrt{\frac{2I}{\beta}} + \frac{w_0}{w}U_{TH} \tag{12}$$

The simple practical realisation of such an amplifier being an integrated circuit realised in the CMOS technique has been shown in Fig. 7.

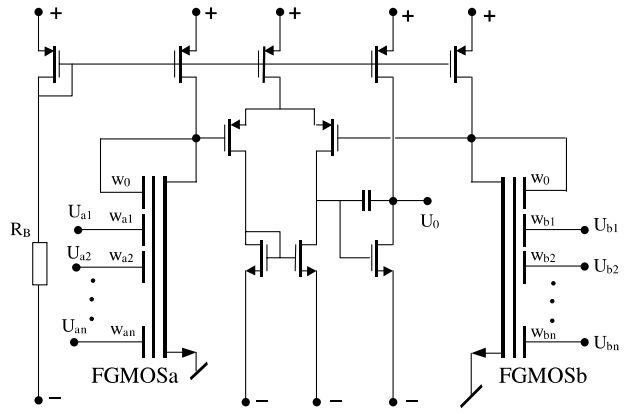


Fig. 7. MIOA simple practical realisation in the CMOS technique with a use of two FGMOS transistors

## 5. Multiple-input OA with FGMOS transistors working in non-saturation region

If differential current amplifier with voltage output and transconductance $R_m$ has been connected to the pair of FGMOS transistors from Fig. 3 working in non-saturation

region in the way presented in Fig. 8, then multiple-input voltage amplifier is obtained. [8]

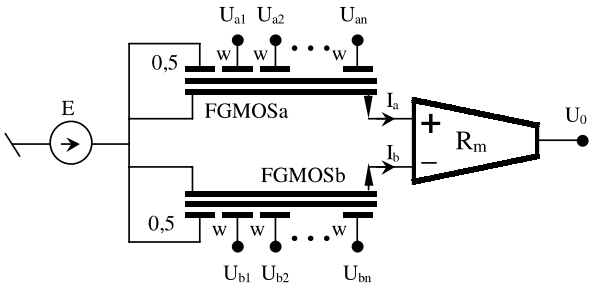


Fig. 8. Multiple-input OA with a pair of FGMOS transistors working in non-saturation region

For the same weight value of all input terminals it is described by the dependence:

$$U_0 = w\beta E R_m \left( \sum_{k=1}^{n} U_{ak} - \sum_{k=1}^{n} U_{bk} \right). \tag{13}$$

In order that transistors work in the triode region each of them must fulfil the inequality:

$$\sum_{k=1}^{n} U_k \geqslant U_G = \frac{1}{w}\sqrt{\frac{I_D}{2\beta}} + \frac{U_{TH}}{2w}. \tag{14}$$

In order to obtain linear transition function also for voltage lower then limit voltage $U_G$, it is possible to apply two pairs of complementary FGMOS transistors powered by E voltage with opposite sign and with compensated threshold voltage $U_{TH}$. The possible structure of practical integrated circuit of MIOA realised in CMOS technique has been presented in Fig. 9 [6], beside which compensation voltage should have value:

$$|U_k| = U_{TH}/w_k. \tag{15}$$

## 6. MIFGMOS transistor as floating linear controlled resistor

For floating gate MOS transistor with four control terminals, operating within the non-saturated region, the dependence (4) describing it, is rearranged to the following form:

$$\frac{I_{DS}}{\beta} = (w_1 U_{G1} + w_2 U_{G2} + w_3 U_{G3} - U_S + w_T U_T + \\ + U_{TH})(U_D - U_S) - \frac{1}{2}(U_D - U_S)^2. \tag{16}$$

Assuming: $w_T U_T = U_{TH}$, $U_{G1} = U_C$, $U_{G2} = U_D$, $U_{G3} = U_S$, $w_2 = w_3 = 0.5$ and $w_1 = w_C$, the following relation is obtained:

$$R_{DS} = \frac{U_D - U_S}{I_{DS}} = \frac{1}{\beta w_C U_C}. \tag{17}$$

That relation describes a theoretical model of floating linear resistor, adjustable by input voltage $U_C$ (in Fig. 6).

The model of controlled floating resistor with one MIFGMOS transistor, shown in Fig. 10, cannot be practically realised, since the sum of all input weights of that transistor is always less them unity therefore whichever two of then cannot be equal to 0.5 at the same time. So, in order to realise it practically, additional amplifiers compensating lowered values for weight $w_2$ and $w_3$ should be inserted between terminals $D$ and $S$ and input gates $G_2$ and $G_3$. Practically, it can be done by means of one am-

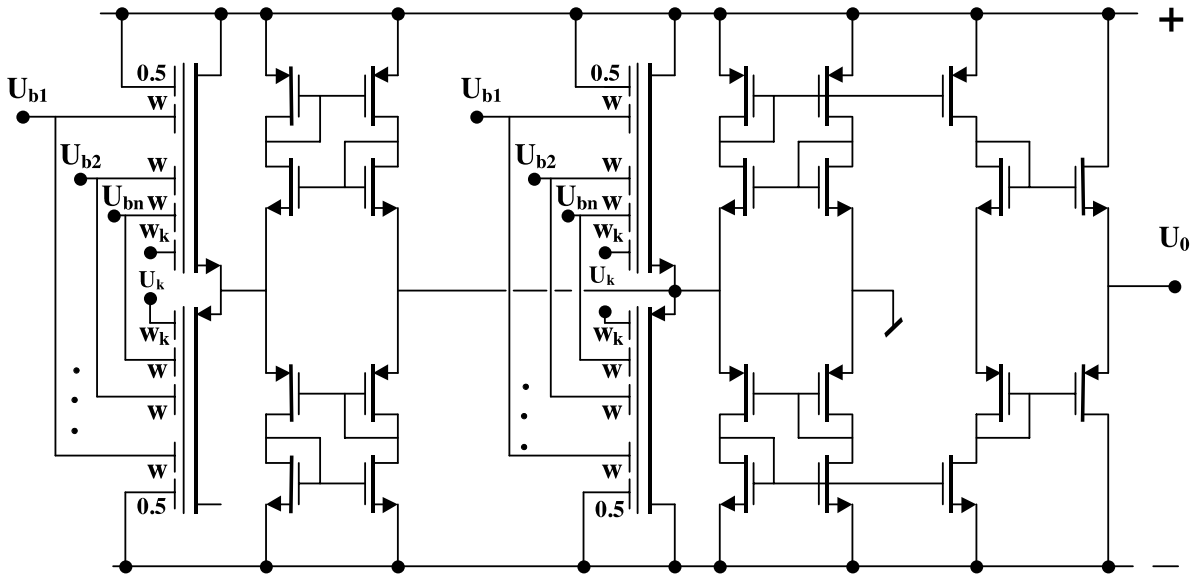


Fig. 9. MIOA practical realisation with a complementary pair of FGMOS transistors working in the triode region

plifier as in Fig. 5 but with two summing inputs. However MIFGMOS transistor can be applied in the version with three terminals controlling the gate. In this case practical circuit of controlled resistor, presented in Fig. 11, is obtained.

The current between $X$ and $Y$ terminals is described by the following relation:

$$I_{XY} = \beta w_C U_C (U_X - U_Y) + \beta A (U_X - U_Y) - \frac{\beta}{2}(U_X - U_Y)^2 \tag{18}$$

in which:

$$A = \frac{w_0}{w_2}\sqrt{2}\left(\sqrt{\frac{I_2}{\beta_2}} - \frac{w_0}{w_1}\sqrt{\frac{I_1}{\beta_1}}\right) + \frac{w_0 w_p w_X}{w_1 w_2} U_X + \frac{w_0 w_p w_Y}{w_1 w_2} U_Y. \tag{19}$$

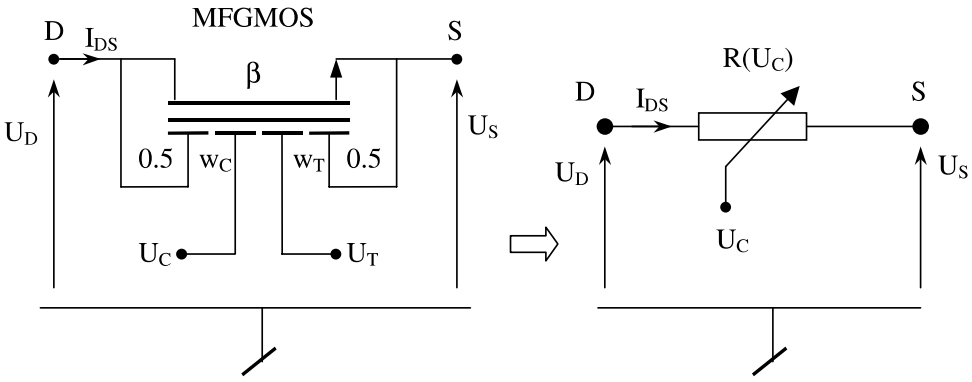


Fig. 10. Theoretical model of floating linear resistor voltage controlled, using MIFGMOS transistor

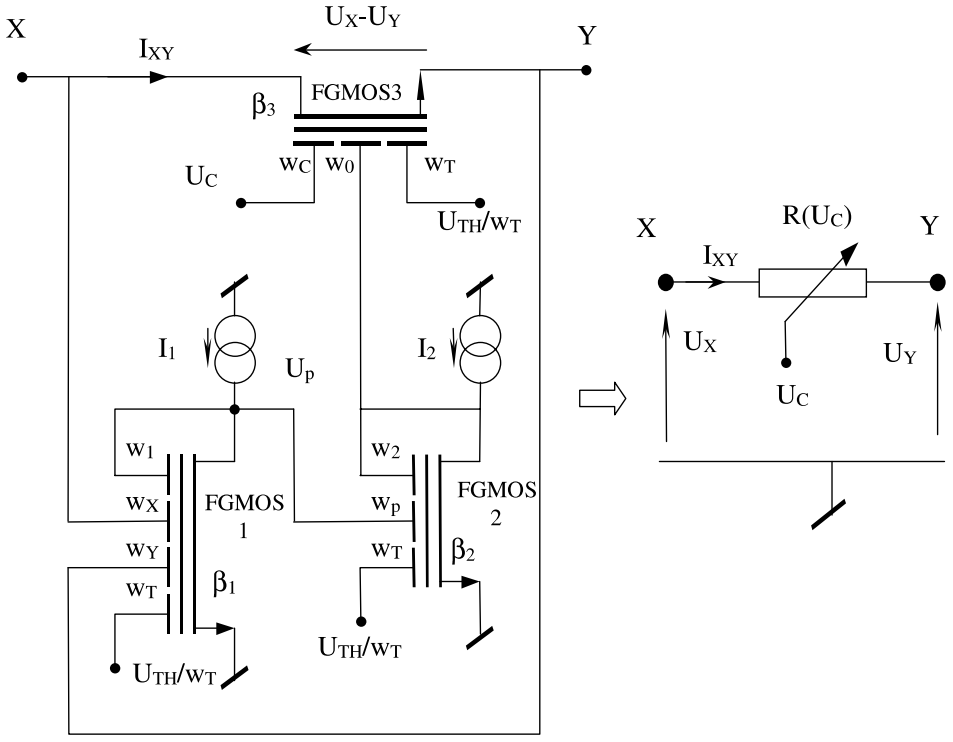


Fig. 11. Practical circuit of floating linear controlled resistor with three MIFGMOS transistor

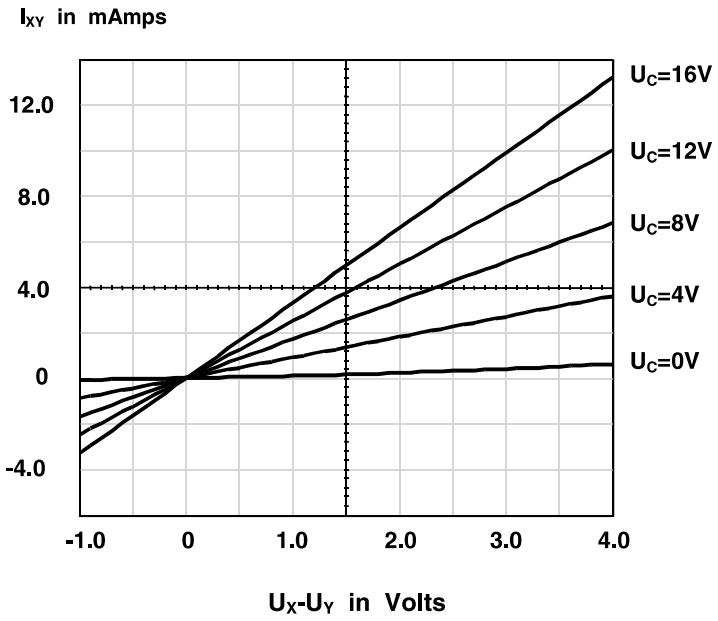


Fig. 12. Current changes for floating resistance $R_{XY}$ versus voltage $U_X - U_Y$ for various values of control signal $V_C$, obtained by SPICE simulation

In order to obtain linear control, MIFGMOS1 and MIFGMOS2 transistors must operate within saturated region, MIFGMOS3 within non-saturated region and at the same time the following dependencies must occur:

$$\frac{w_p}{w_1} = 1 \quad \text{and} \quad \frac{w_0 w_p w_X}{w_1 w_2} = \frac{w_0 w_p w_Y}{w_1 w_2} = \frac{1}{2} \tag{20}$$

In Figure 12 changes of current $I_{XY}$ versus $V_X - V_Y$ for various values of control signal $V_C$, have been presented. The simulation has been carried out in SPICE for: $w_1 = w_0 = w_p = 0.2$, $w_X = w_Y = 0.1$, $w_2 = 0.04$, $I_1 = I_2 = 1$ mA and $\beta_1 = \beta_2 = \beta = 10^{-4}$ A/V$^2$.

## 7. Conclusion

Realisations of voltage amplifiers using multiple-input floating gate field-effect transistors MIFGMOS are quite simple and at the same time there is the possibility to obtain parameters which are quite close to the ones intended in given input signal range. Conception of realisation of floating linear voltage controlled resistor presented is simple and requires only three MIFGMOS transistors and two current sources. It operates within sufficiently wide range of terminal voltages and control voltages and owing to it, can find its applications in many adjustable and adaptation circuits.

## References

[1] Y. Berg, O. Naes and M. Hovin, "Ultralow-voltage floating-gate transconductance amplifier", *IEEE International Symposium on Circuits and Systems*, III, 347–350 (2000).

[2] *IEEE Trans. on CAS-II. Special issue on floating-gate devices, circuits, and systems*, No. 1, January 2001.

[3] L. Topór-Kamiński, „Komputerowa symulacja układów z tranzystorami MOS ze swobodną bramką", *VI Konferencja Naukowo-Techniczna Zastosowania Komputerów w Elektrotechnice*, Poznań, 2001.

[4] L. Topór-Kamiński, „Proste wzmacniacze napięciowe z tranzystorami MOS o bramce swobodnej", *XXIV IC-SPETO*, 409–414 (2001).

[5] J. J. Chen, S. I. Liu and Y. S. Hwang, "Low-voltage single power supply four-quadrant multiplier using floating-gate MOSFETs", *IEE Proc.-Ciscuits Devices Syst.* 145, 40–43 (1998).

[6] L. Topór-Kamiński, „Wielozaciskowy napięciowy WO z tranzystorami MOS o bramce swobodnej", *Krajowa Konferencja Elektroniki*, Kołobrzeg, 205–210 (2002).

[7] L. Topór-Kamiński, „Tranzystor polowy MOS o bramce swobodnej ze sprzężeniem wewnętrznym", Zgłoszenie patentowe nr P 353815 z dnia 10.05.2002.

[8] L. Topór-Kamiński and P. Holajn, „Tranzystory MOS o bramce swobodnej w obszarze nienasycenia współpracujące ze wzmacniaczami operacyjnymi", *VII Konferencja Naukowo-Techniczna Zastosowania Komputerów w Elektrotechnice*, Poznań, 63–66 (2002).