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Micro and nano structurization of semiconductor surfaces

A. GÓRECKA-DRZAZGA*

Faculty of Microsystem Electronics and Photonics, Wrocław University of Technology, 11/17 Janiszewskiego Str., 50-372 Wrocław

Abstract. The techniques of micro and nano structurization of surfaces of various materials are utilized in electronics and medicine. Such procedure as wet and dry etching allows to fabricate protruded or recessed micro and nanostructures on the surface. In the paper some examples of utilization of a surface structurization, known from literature, are described. Some structurization methods and experimental results for fabrication of the arrays of sharp microtips are presented. Wet and/or dry etching, and thermal oxidation process were used to form the arrays of sharp gated and non-gated, protruded or recessed silicon microtips on silicon wafer. For the first time, the arrays of silicon carbide (SiC) microtips on glass wafer have been produced by use of the transfer mold technique. Arrays of sharp microtips are used as field electron emission cathodes for vacuum microelectronics devices. Some electron emission measurements for these cathodes have been carried out. New application of silicon microtips array in biochemistry has been tested with satisfactory results.

Key words: silicon tips, SiC tips, transfer mold technique, field emission, FEA.

1. Introduction

Micro and nano structurization of dielectric, metallic and semiconductor surfaces is used for a modification of such surface properties as topography, roughness, light reflectivity, chemical activity, and biocompability. These features have a potential use in many branches of science and technology, especially in electronics and medicine. It is also possible to form surfaces with many protruded or recessed micro and nanostructures, which can be applied in special miniaturized devices.

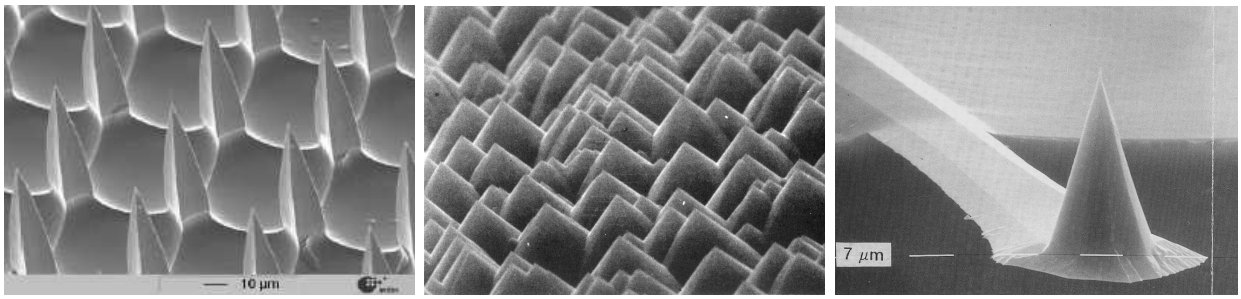
Thanks to quick development of microelectronics and microengineering techniques micro and nano structurization of materials surface became possible. Dry and wet etching methods provide new types of medical application, e.g. microfabrication of microneedle arrays for measurements of biopotentials and transdermal delivery of drugs in non-painful manner (Fig.1a) [1,2]. The mechanical, chemical and morphological characteristics of materials are crucial with respect to resulting tissue response and implant durability. It has been stated that technique of ion sputtering can modify surface of biocompatible materials by enhancing cells attachment to the implanted material [3].

Standard technique for fabricating solar cells on silicon wafers uses silicon (Si) wafers with textured surfaces [4]. Any "roughening" of the surface reduces reflection by increasing the chances of reflected light bouncing back onto surface, rather than out to the surrounding air. Thus surface texturization is used to minimize reflection and improve the efficiency of cells, with targets aiming towards the currently accepted theoretical limit of about 30%. Wet etching along the faces of the crystal planes can texture the surface of crystalline silicon uniformly. The crystalline structure of silicon results in a surface made up of pyramids, if the surface is appropriately aligned to the internal atoms (Fig. 1b).

Surface structurization is also applied in MEMS (Micro-Electro-Mechanical Systems). A sharp wet etched silicon tip attached to a cantilever-like spring is used as a probe for scanning force microscopy [5] (Fig. 1c). Intentionally modified surfaces are used in new devices with quantum structures, permeable membranes and in photo luminescent and electro luminescent devices [6]. Surface roughening is very effective to enlarge intensity radiated from a semiconductor light emitting diodes (LED). Surface structurization of SiC and Ga-containing semiconductors (Fig. 2) has been realized by dry etching in high-frequency reactive plasmas [7].

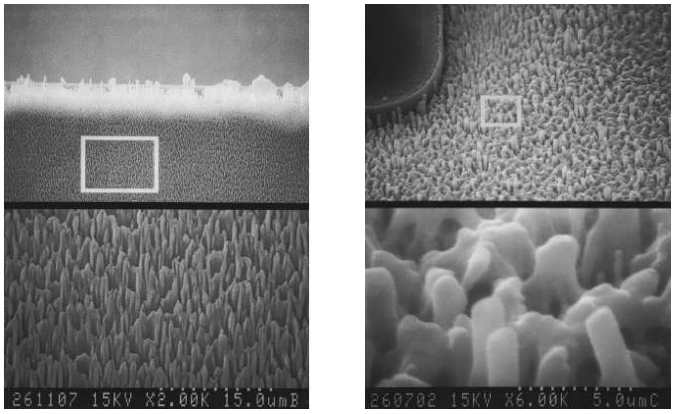
The electrochemical etching of silicon has been utilized as a structurization technique to obtain nano and micro porous surfaces [8]. Recently, a porous silicon and porous silicon dioxide layers has been used in μ-TAS (Micro Total Analysis Systems) for modification of chemical and electrical properties of surface microchannels for gas and/or liquid flow (Fig. 3). Porous silicon dioxide layer was fabricated to form electrically insulated microchannels in silicon [9]. Silicon pillars covered with porous layer have been used for increasing of gas-liquid contacting surface in micromixer [10] and surface activity in enzyme microreactor [11]. Porous silicon-glass microchannel has been applied as chromatography microcolumn (Fig. 4) for separation of the aromatic hydrocarbons [12]. Recently, silicon chip with porous surface has been used in matrix-free desorption/ionization mass spectrometry (MALDI MS). It was discovered that porous silicon dioxide spots make possible to identify the low-mass bioactive species as proteins and peptides [13].

*e-mail: anna.gorecka-drzazga@pwr.wroc.pl



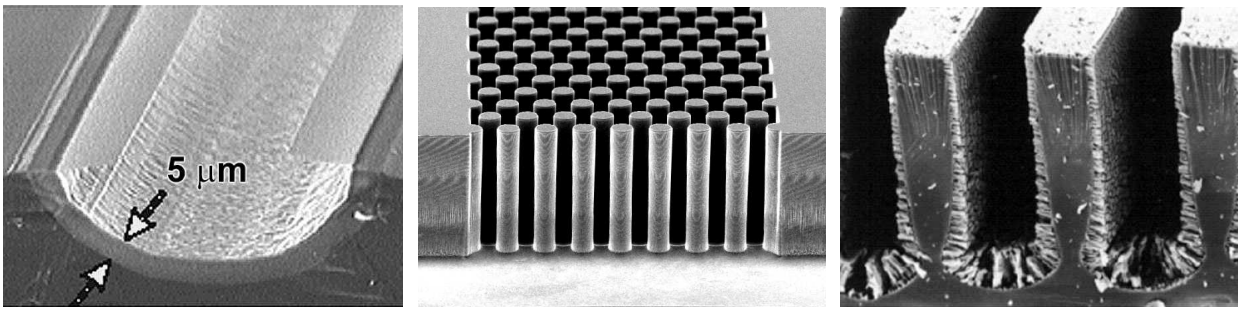
(a) (b) (c)

Fig. 1. Texturized silicon surfaces: microneedle array formed by dry etching (a) (after Ref. 2), solar cell, pyramids 10 µm high formed by wet etching (b) (after Ref. 4), silicon tip formed by wet etching for scanning force microscopy (c) (after Ref. 5)



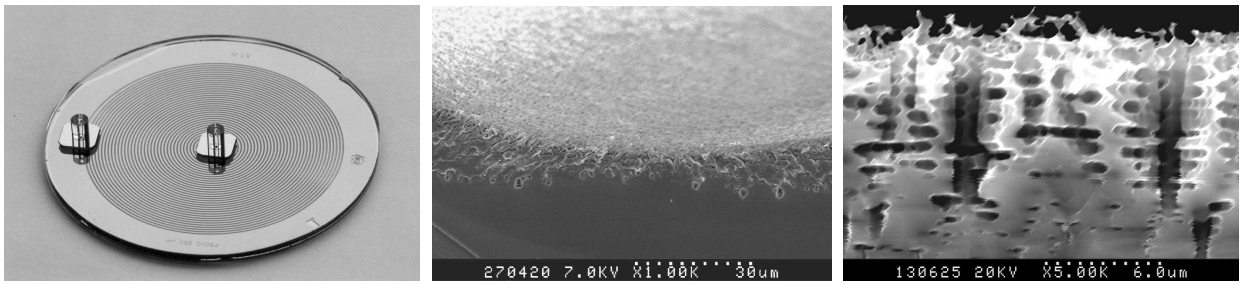
(a) (b)

Fig. 2. Structurized surfaces: GaP roughed in reactive plasma containing $Cl_2/O_2/Ar$ (a), SiC roughed in reactive plasma containing $CF_4/Cl_2/O_2$ (b) (after Ref. 7)



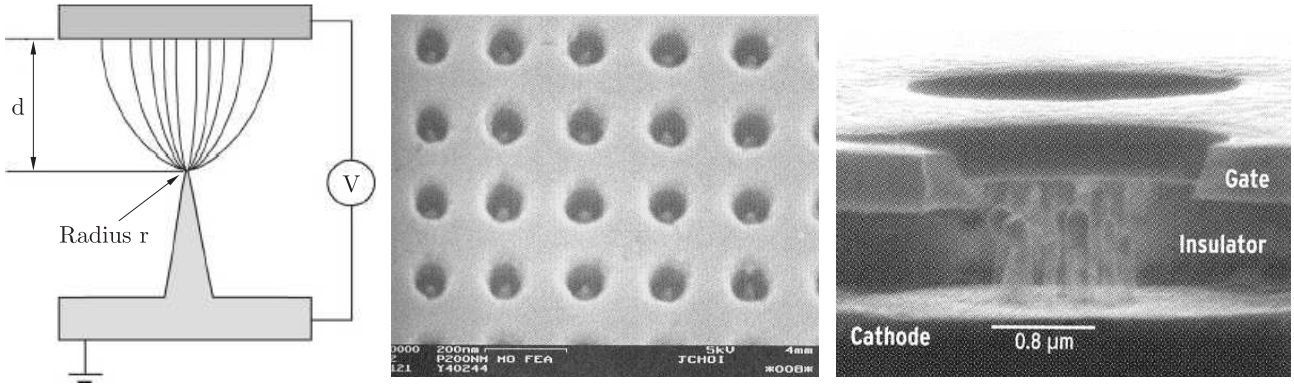
(a) (b) (c)

Fig. 3. Fragments of the silicon µ-TAS devices with porous layers: electrically insulated microchannel (a) (after Ref. 9), micromixer (b) (after Ref. 10), enzyme microreactor (c) (after Ref. 11)



(a) (b) (c)

Fig. 4. Silicon-glass microcolumn (a), SEM pictures of porous silicon dioxide on the channel bottom (b) (after Ref. 12)



(a) (b) (c)

Fig. 5. Illustration of field electron emission from sharp tip (a), Spindt-type cathode array – molybdenum cones surrounded by metallic extraction electrode (gate) (b) (after Ref. 17), gated carbon nanotubes cathode (c) (after Ref. 18)

Micro and nano structurization of surface has been used in vacuum microelectronics since 1968 [14]. The most representative examples of the microelectronics devices are flat panel displays and miniaturized electron sources for microwaves generators and amplifiers, and spectrometers for space applications [15, 16]. These devices utilize microfabricated low-voltage, high current, field-emission cathodes to obtain electron emission (no external energy supply) (Fig. 5a). Field-emission cathodes contain arrays of sharp microtips and are capable of emitting the current in the range of 10–10^4 Acm^{-2} averaged over the total cathode area. The turn-on voltage for electron emission is very low (from 10 to 200 V) when the sharp microtips has a metal gate (Fig. 5b) [17]. If a metal gate is located about 1 μm from microtip, and the radius of a microtip summit equals about 10 nm, it is possible to generate an electrical field larger then 5×10^7 V/cm, what is necessary for electron field emission. Novel developed cathodes are made from nanomaterials as nanotubes (Fig. 5c) [18], nanocompositions and nanostructurized thin layers [16].

The works on surface structurization for vacuum microelectronics devices started in Faculty of Microsystem Electronics and Photonics of Wroclaw University of Technology in 1991 (in this time – Faculty of Electronics) [19]. The "Silicon Micromechanics and Microengineering Group" was engaged in works on technology of the silicon micromechanical sensors and actuators. With the help of the experiences captured in these technological researches the fabrication procedures of microtips have been developed. Crucial research challenge was to fabricate millimeter-size Si chip with hundreds of thousands micrometer-size tips, each with nanometer-size summit. In this paper some structurization methods and experiment results for fabrication of the arrays of the sharp microtips have been presented. Wet and/or dry etching, and thermal oxidation process were used to form the arrays of sharp gated and non-gated, protruded or recessed silicon microtips on the silicon substrates. For the first time, the arrays of silicon carbide (SiC) microtips on glass wafer were produced by use of the transfer mold technique.

2. Experiments and results

2.1. Silicon microtips. Silicon field-emission arrays (FEAs) became important type of cathodes for vacuum microelectronics devices. These microstructures are fabricated by use of following methods:

- Wet, anisotropic or isotropic silicon etching (aqueous alkaline solutions: potassium hydroxide, ethylene diamine pyrochatechol, tetramethylammonium hydroxide; aqueous acid solutions: nitric acid and hydrofluoric acid),
- Dry, anisotropic or isotropic silicon etching (ion beams, plasmas),
- Transfer mold technique.

The step-by-step procedure of silicon surface structurization by use of wet etching is presented in Fig. 6. The silicon substrates with resistivity 3 Ωcm, (100) and (111)-oriented, were used. First, silicon substrate was wet thermal oxidized (1100°C, 3 hours) and thermal oxide masks, 1 μm thick, were photolitographically patterned as 3, 8, 12, 15 μm diameter circles. Then, properly shaped silicon precursors were formed by wet isotropic etching in HNO_3:HF:CH_3COOH = 25:3:10 (NHA) water solution, at room temperature (Fig. 6b, 6c).

Next, the microtips sharpening process was carried out by thermal oxidation of silicon precursors (950°C, 2.5 h). Due to the Grove-Deal's effect [20], thicker oxide layer is generated on flat surface than on concave or convex surface. As a result, arrays of 3 to 5 μm high microtips with summit radius less than 10nm have been fabricated (Fig.7) [21]. Final results of sharpening process depend on quality of photolithography and uniformity of silicon etching on the whole substrate surface. In the place where the mask reached, the characteristic depressed area round the base of the microtip was observable. Width of the top precursors bigger then 0.5 μm, makes impossible properly sharpening of the microtips. It has been observed that shape of the microtips clearly depends on the crystallographic orientation of the substrate (Fig. 7). The wet etching process known as isotropic in a macro-scale has appeared to be anisotropic in a micro-scale. SEM pictures have shown different shapes for microtips formed (in the same solution) on (100) and (111) silicon surface.

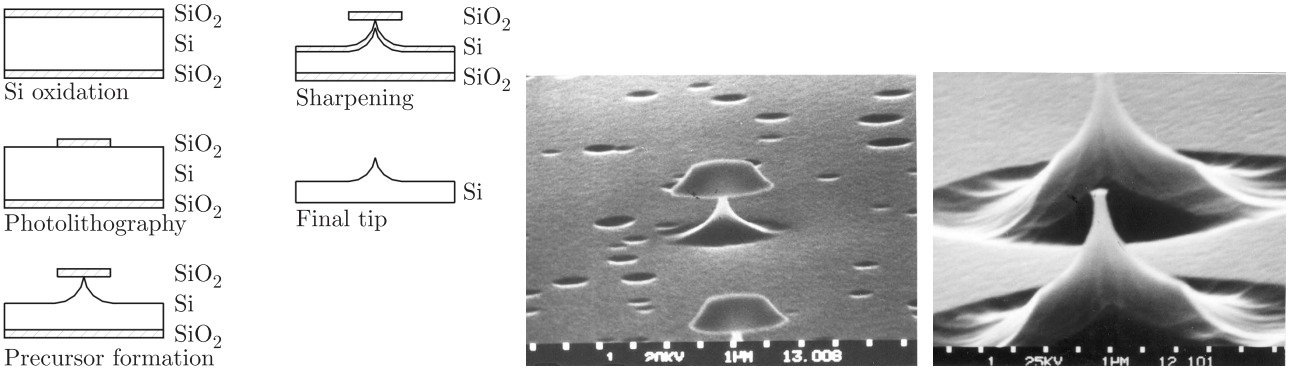


Fig. 6. Main technological steps of protruding tips fabrication (a), SEM picture of (100) Si precursor with dioxide mask (b), SEM picture of Si precursors after silicon dioxide mask removing (c)

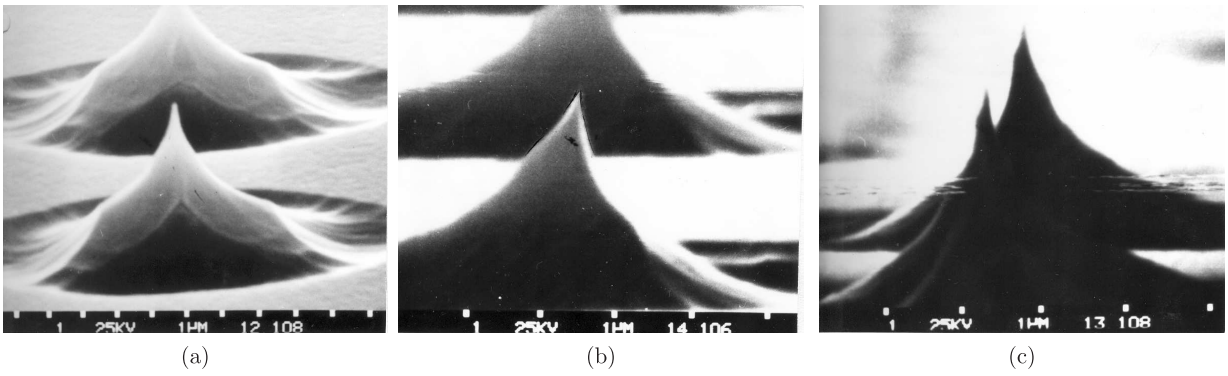


Fig. 7. SEM pictures of micro tips after thermal oxidation: (100) silicon (a), (111) silicon (b) and (c) (after Ref. 21)

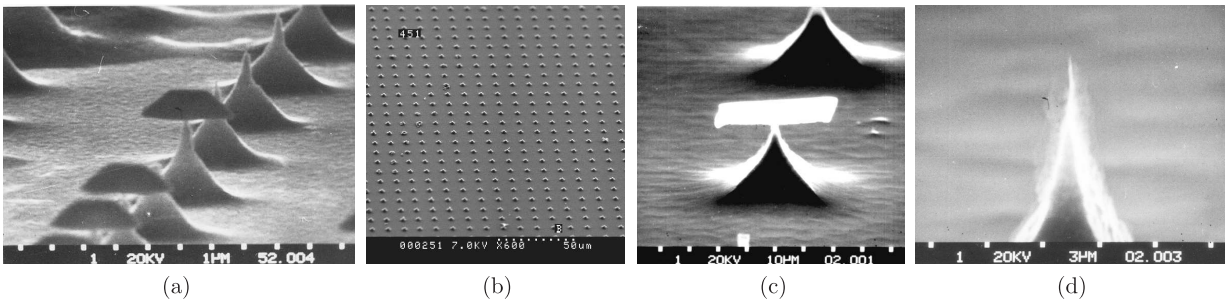


Fig. 8. Silicon microtips fabricated by plasma etching: tips with SiO_2 masks, p = 4×10^{-3} kPa, SF_6 = 12 sccm, supply power P_{RF} = 100 W (13.56 MHz), Si (111) (a), array of tips without masks (b), tip with Al mask, p = 2×10^{-2} kPa, SF_6 = 12 sccm, P_{RF} = 150 W, Si (100) (c), summit of microtip after Al mask removing (d) (after Ref. 22)

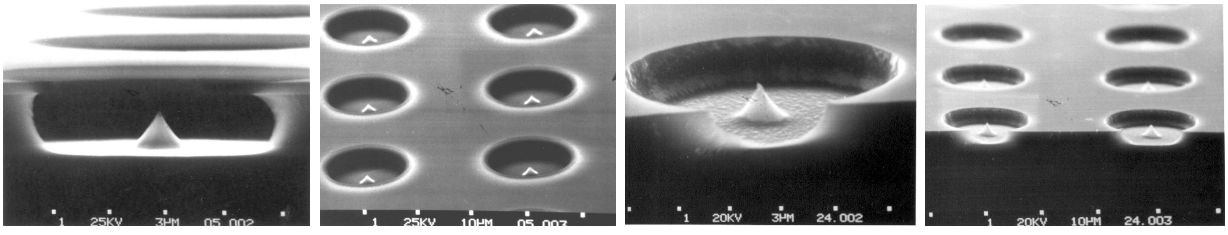


Fig. 9. Recessed silicon microtips obtained by connected techniques: dry etching p = 3×10^{-3} kPa, SF_6 = 24 sccm, Cl_2 = 6 sccm, P_{RF} = 150 W followed by wet etching in NHA, Si (100) (a) and (b), dry etching, p = 3×10^{-3} kPa, SF_6 = 24 sccm, Cl_2 = 6 sccm, P_{RF} = 150 W followed by thermal oxidation, Si (100) (c) and (d)

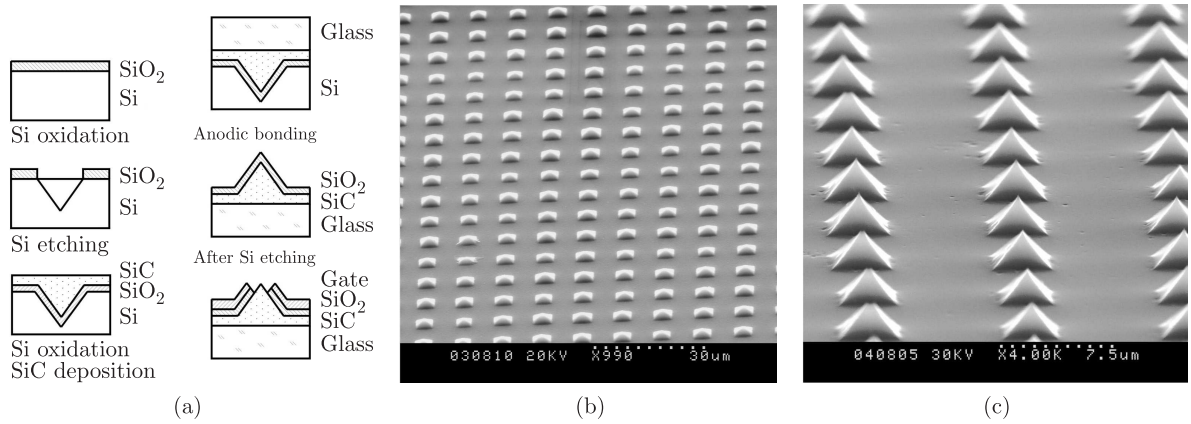


Fig. 10. SiC FEA step-by-step fabrication process (a), SEM picture of SiC FEA before silicon dioxide removing, 5^{th} step in the figure on left (b), SEM picture of SiC FEA after silicon dioxide removing (c)

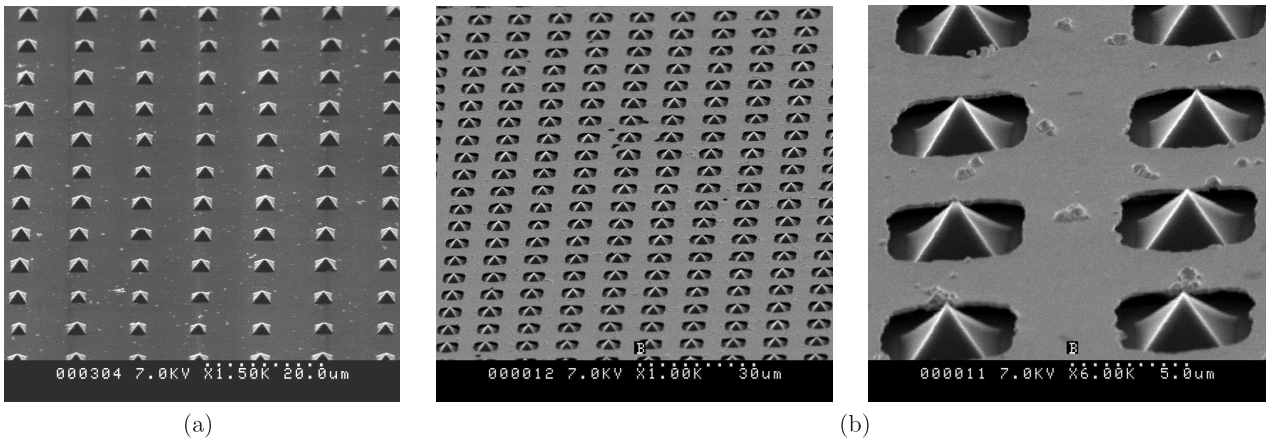


Fig. 11. SEM picture of non-gated mold-type SiC FEA (a), SEM pictures of gated mold-type SiC FEA (b)

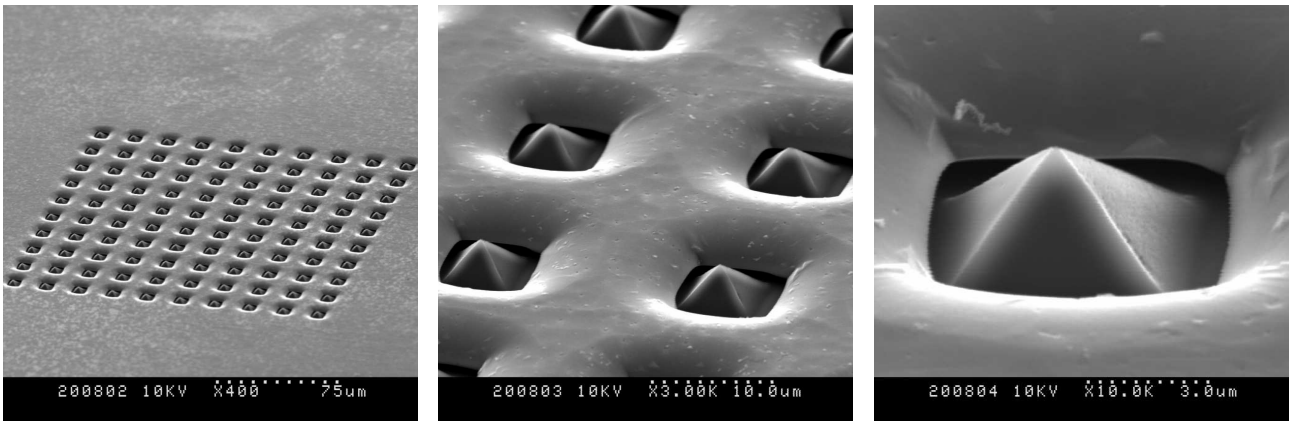


Fig. 12. SEM pictures of the SiC microtips with 7 μm-high boron doped gate support

Silicon surface micro structurization was studied by use of the dry etching method. The processes of plasma etching to obtain microtips precursors were carried out in RIE-type (Reactive Ion Etching) device (GIR-300 Alcatel), with SF_6, SF_6/O_2, SF_6/Cl_2 gas mixtures [22]. Precursors were etched out under the silicon dioxide or aluminium mask to top width equal about 0.5 μm, and sharpened by use of a thermal oxidation or/and wet isotropic etching (Fig. 8). It is possible to form an array of microtips, which are located under a silicon surface. The satisfactory results can be obtained then different described techniques are connected. In this case the geometry of tips was similar, and better repeatability was obtained (Fig. 9).

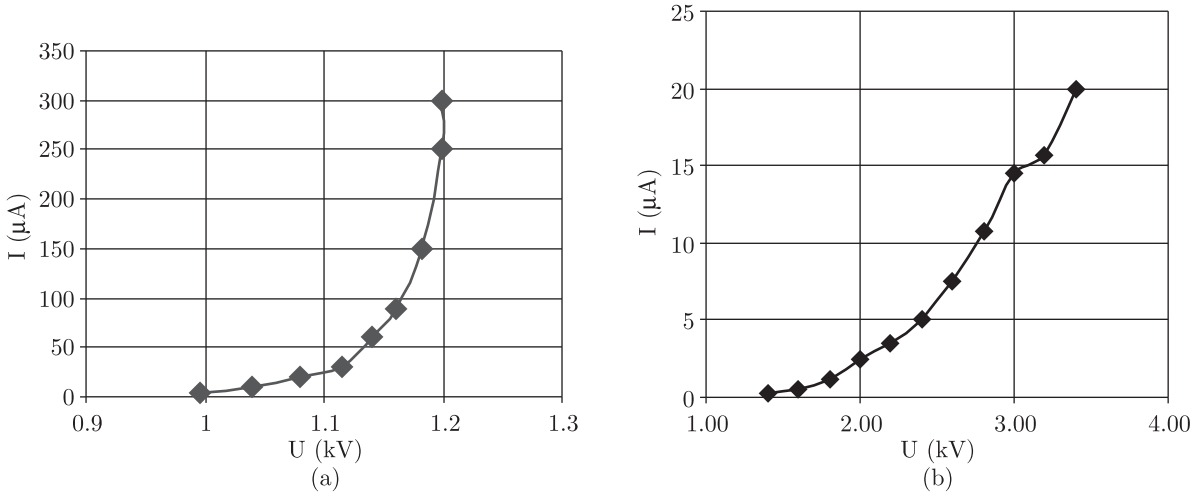


Fig. 13. Results of measurements of field emission current for electron sources: array of silicon microtips covered with a thin layer of platinum (a), array of SiC mold-type microtips (b)

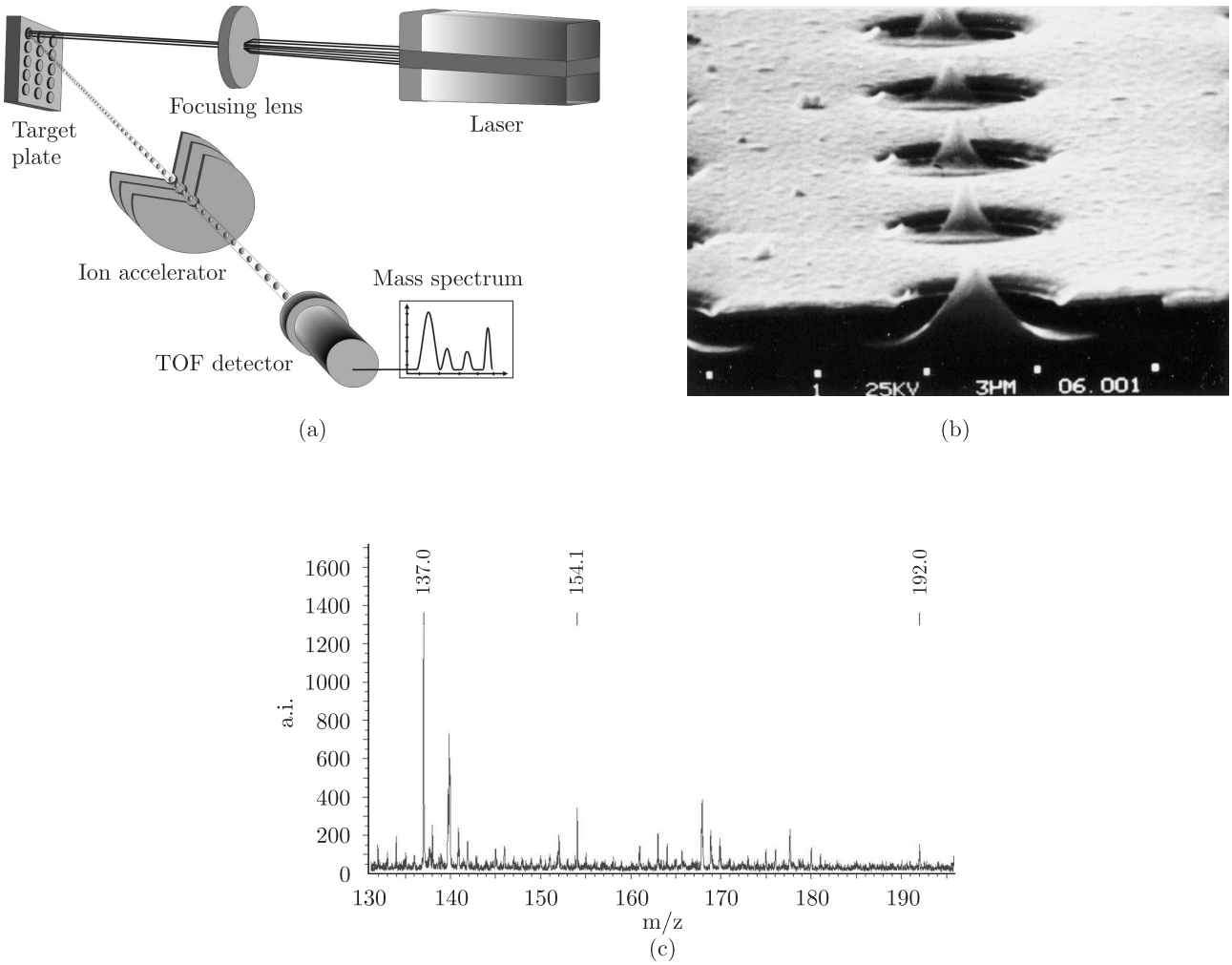


Fig. 14. Schematic view of MALDI TOF MS equipment (a), SEM picture of gated silicon microtips not covered with a bio-sample (b), mass spectrogram of dopamine 65 pmol per spot Molecular ion at a m/z of 154.1 and its fragment at 137.03 may be seen (c)

2.2. SiC mold-type microtips. The transfer mold technique offers a unique possibility to transfer structurized thin layer from silicon substrate to glass wafer. This method allows fabricating micro and nano structurized surfaces for many materials, for example: diamond, poly-Si, TiN, LaB_6, [23,24]. The arrays of microtips made from SiC have been produced for the first time by use of this technique [25]. In the mold technique "negative" replicas of microtips are anisotropically wet etched in (100) oriented, monocrystalline silicon substrate (Fig. 10). Reversed pyramid-like cavities are filled with an emissive layer, and Si substrate is anodically bonded to Pyrex-like glass wafer. Finally, unnecessary silicon substrate is removed by wet anisotropic etching in alkaline solution. SiC FEAs have been fabricated in two versions: as non-gated arrays (Fig. 10c and Fig. 11a) and as gated arrays (Fig. 11b). Gate is a metallic extraction electrode, which decreases turn-on voltage for electron field-emission. On insulating SiO_2 layer, which cover the SiC pyramids, the metallic layer is deposited and micrometer-size windows are opened at the summit of tips by wet or dry etching.

Works on the transfer mold technique for SiC FEAs resulted in a new technological possibility. Selective heavy boron diffusion to a silicon allows generating a few micrometer high regions. All SiC microtips are surrounded by boron-doped region, which may serve as a gate or anode support (Fig. 12). The device is formed in multi-step fabrication process with using thermal oxidation, wet etching, boron diffusion and anodic bonding [26].

3. Applications

Described silicon surface structurization procedures have been utilized for fabrication of the miniaturized vacuum microelectronics devices. Arrays of 2500 silicon microtips (on area 1 mm^2) covered by platinum thin layer (30 nm) were tested as electron sources in diode configuration [27]. Anode was located about 25 μm above the structurized cathode. Test structures were placed in vacuum apparatus in oil-free atmosphere under vacuum better than 10^{-8} kPa. The resulted current-voltage characteristic is shown in Fig. 13a. The maximal current equal 350 μA was obtained.

Electron field-emission from arrays of about 10 thousand SiC microtips produced by the transfer mold technique have been studied in diode configuration [25]. Nickel flat anode was located 160 μm above mold-type cathode. The efficient emission from the microtips array has been obtained (Fig. 13b).

For the first time, arrays of gated silicon microtips have been used for laser desorption/ionization of bio-samples for time-of-flight mass spectrometry (TOF MS) [28]. Thousands of gated silicon microtips, grouped in spots of varying size, were fabricated on a silicon wafer (Fig.14b). This wafer served as a new platform for TOF MS measurements made with use of the standard equipment (MALDI TOF Reflex IV mass spectrometer, Bruker Saxonia) (Fig. 14a). Carried out tests documented clearly that mass spectrograms obtained by the application of gated microtips array spots make possible to identify low-mass bio-samples such as a dopamine. It was not possible for MALDI TOF with standard platform.

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