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A Method to Support Diagnostics of Dynamic Faults in Networks of Interconnections

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***Abstract*—The article is devoted to the method facilitating the diagnostics of dynamic faults in networks of interconnection in systems-on-chips. It shows how to reconstruct the erroneous test response sequence coming from the faulty connection based on the set of signatures obtained as a result of multiple compaction of this sequence in the MISR register with programmable feedback. The Chinese reminder theorem is used for this purpose. The article analyzes in detail the various hardware realizations of the discussed method. The testing time associated with each proposed solution was also estimated. Presented method can be used with any type of test sequence and test pattern generator. It is also easily scalable to any number of nets in the network of interconnections. Moreover, it supports finding a trade-off between area overhead and testing time.**

***Keywords*—network of interconnections, system-on-chip, diagnostics, MISR, compaction, signature, Chinese remainder theorem**

I. Introduction

NANOMETRIC technologies that are currently in common use make dynamic faults, such as delay faults and crosstalks, a significant group of faults that affect all transmission paths [2, 1, 13]. Such faults are particularly detrimental to long links between digital modules of complex digital systems on chips (SoC).

The diagnostic phase and investigation of reasons for faults detected in integrated systems need the knowledge on actual values of faulty signals at specific points of the system, for instance at inputs of flip-flops that make up the scan-path of the system or on interconnections between digital modules of SoCs. The topics associated with location of scan-path flip-flops assigned to store faulty values of test responses received from the system under test have already been thoroughly analyzed in such studies as [15, 20]. The key assumption adopted for the both studies consists in the fact that only small number of scan-path flip-flops records faults in test responses received from the system. It is just the opposite situation in case of interconnections between digital modules of SoCs. Even insignificant number of dynamic faults or combinations of static and dynamic faults may lead to very large number of errors in serial vectors of responses received from tests of interconnections. It is illustrated by the following example.

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Example 1

Let us assume that an interconnection line is stimulated by a serial test vector with the length of 1000 bits. Let us also assume that the test vector contains 100 rising and 100 falling edges of the test signals. If a delay fault affects the both edges, the serial vector of test responses recorded at the far end of that interconnection shall comprise at least 200 errors (i.e. bits of incorrect values). What is worse, also additional errors may appear due to crosstalks since the interconnection line can be a victim of a crosstalk interference. Also simultaneous presence of both static and dynamic faults can entail significant number of errors, e.g. in case of shorts between transmission lines when a delay fault appears on at least one of these lines. ♦

Unfortunately, the method suggested in [20] needs to collect a substantial number of signatures to identify many of the errors in sequences of test responses. It is associated with the requirements imposed by the corrective Reed-Solomon code [16] used by the method. Thus, the method is well-suitable for identification of those scan-path flip-flops that store erroneous bits of test response sequences received from the system under test but is completely useless for diagnostics of dynamic faults appearing on interconnections. To correctly identify delay faults in interconnections from Example 1 by means of the solution suggested in [20] it is necessary to collect as many as 400 signatures. It is also the number of test repetitions, i.e. how many times the test sequence should be delivered to inputs of the network of interconnections. Should long test sequences with high diagnostic resolution are used the test duration may extend beyond the acceptable limits.

The solution disclosed in [15] needs to collect even more signatures than is stipulated in [20]. In addition, the suggested method is a probabilistic approach that is incapable to guarantee that all erroneous bits are identified in sequences of test responses received from the network of interconnections.

The further part of this study is structured in the following way: Chapter 2 is devoted to summarize previous studies of the author related to testing and diagnostics of networks of interconnections in SoCs. The next chapter comprises an outline of theoretical backgrounds for the method that is applied to find out the response to test sequence for interconnections with use of a Chinese remainder theorem. The subsequent chapter, i.e. Chapter 4, is dedicated to hardware implementation of the test method in question. Chapter 5 discloses the scenarios for testing and diagnostics of faults in networks of interconnections. Finally, the recapitulation of the study and final conclusions are summarized in Chapter 6.

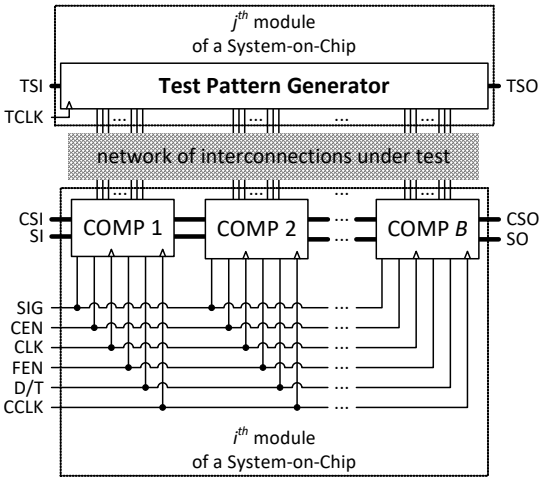

Fig. 1. Block diagram of the hardware used to test the network of connections between the digital cores of a system-on-chip

II. PREVIOUS STUDIES

The baseline paper [11] discloses an innovative method for detection, localization and identification of static faults in networks of interconnections. The methods is based on the concept of a normalized signature with the value that depends exclusively on the compacted sequence of test responses but is irrelevant to the input of the MISR register where the sequence is supplied. Owing to that property the normalized signatures enable easy identification of transmission lines that are stuck to low or high levels as well as the lines shorted one to another. The schematic diagram of the IBIST structure applied to the method in question is disclosed in Fig. 1. The diagram shows that the compactor module for a network of v interconnections is made up of B number of n-bit COMP modules whilst each of the COMP modules (Fig. 2a) comprises two key components: the IET-MISR compactor register and the Control Shift Register (CSR). The IET-MISR compactor is made up of cells that can operate as either D or T flip-flops, where the cell structure is depicted in Fig. 2b. The D/T signal is used to select the flip-flop mode of operation (*D/T flip-flop type*). The test and fault localization procedures involve operation of these flip-flops in the T-mode (D/T=1) whilst operation of the IET-MISR register in the scan mode consists in serial shift of the register content, i.e. each its cell performs as a D-type flip-flop (D/T=0). Such a solution simplifies setting of the compactor initial state and withdrawal of the result signature as well as makes it easier to integrate the compactor with a scan path or other tools designed to facilitate testing of SoCs compliant with the IEEE 1500 standard [4]. The additional signal FEN (*Feedback Enable*) makes it possible to open the feedback loop (FEN=0) whilst separate use of D/T and FEN signals enable closing of the feedback loop for both D and T flip-flops, which allows easy testing of the compactor operability. The bit mask designed to enable AND gates at inputs of the IET-MISR register is shifted inside in the serial mode and stored in the CSR register. The CEN (*Compactor Enable*) signal makes it possible to disable all inputs of the IET-MISR compactor register with simultaneous shifting of information both in the compactor and the CSR registers. The AND gate at the compactor input is controlled by means of the SIG (*Serial Input Gating*) signal and enables mutual isolation of individual n-bit COMP modules. Operation modes of the compactor are summarized in Table I.

To speed up the procedure of testing and diagnostics of interconnections as many as three separate scan-paths are provided, i.e. SI...SO, CSI...CSO and TSI...TSO. All scan-paths are operated in parallel. To simplify description of the operation mode three separate clock series CLK, CCLK and TCLK are used, one clock series for each scan path. In practice all these mentioned three scan paths can be controlled by means of a single clock signal and flip-flops furnished with the CE (*clock enable*) input designed to disable the clock signal.

The number of IET-MISR registers necessary to detect and localize of faults with identification of their types is $B=\lceil v/n \rceil$, where v stands for the number of interconnections and n defines the size of the IET-MISR register. Thus, the total length of the register that comprises B number of n-bit IET-MISR registers is $B \cdot n$. Should the number of interconnections v is not a multiple of n the unused inputs of

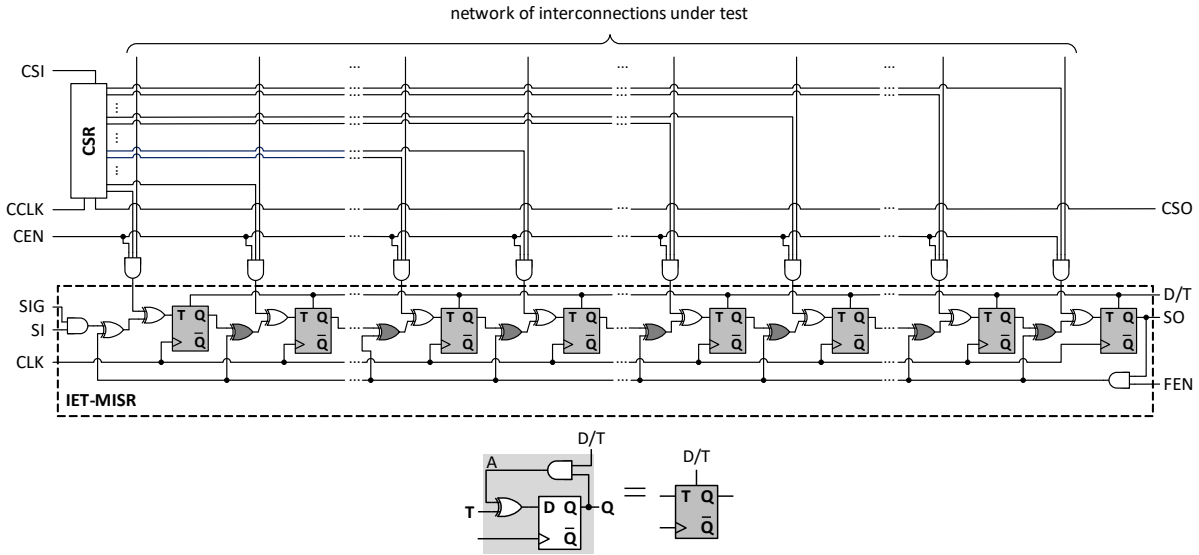

Fig. 2. Schematic diagram for the logics of a single COMP module (a) and the internal structure of the T-type flip-flops used for the compactor design (b)

TABLE I
Operation modes of the compactor register

Operation mode of the compactor register	Register function	FEN	D/T	CEN	SIG	CSR
Serial data exchange with an external tester	Setting of the initial content and reading of the test signature	0	0	0	1	xx...xxx...xx
Parallel compaction simultaneously in all COMP modules	MISR	1	1	1	0	11...111...11
Serial compaction in a single COMP module	SISR	1	1	1	0	00...010...00
Test of the global feedback line	LFSR	1	1	0	0	xx...xxx...xx

the IET-MISR register should be connected to a fixed logic level, e.g. logic zero (low) that enables simplification of the register structure.

Let us notice that the study [11] assumes that an IET-MISR register made up of T-type flip-flops can be used to compact test responses from a network of interconnections under tests and is fully substitutive to the conventional IED-MISR register that comprises only flip-flops of the D type. It results from the fact that the IET-MISR register associated to the primitive polynomial offers benefits in detection of faults as compared to a conventional IED-MISR structure. It happens due to mutual aliasing of error sequences. The more that the feedback structure of any MISR register to be used has no effect to its capability of fault localization and identification of their types.

The method disclosed in [11] offers high flexibility and good scalability. It can be combined with any test pattern generator and owing to modular structure of the MISR register designed to compact test responses it actually enables testing of interconnection networks with practically unlimited size. Its substantial advantages include also the fact that on one hand it supports *at speed* testing and diagnostics of networks of interconnections and on the other hand it enables transfer of collected signatures into an external tester at much lower rates. The concept of normalized signature and the IBIST structure disclosed in [11] made it possible to develop the method enabling unambiguous identification of static faults in interconnections [5, 6] based on application of W1, W0 and J test sequences (the latter is a fragment of test vector sequence produced by the Johnson counter) combined with the three-signature analysis.

The study [12] discloses the method designed to support detection of dynamic faults in interconnections. The method is focused on determination of the response sequence to be received from a defective transmission line and is based in the Chinese remainder theorem and an enhanced IBIST structure from [11]. In [12] the authors paid major attention to disclose theoretical fundamentals of the methods but the issues related to its hardware implementation have been addressed rather superficially. Therefore this study is intended to fill that gap and to comprehensively present the method in details combined with thorough analysis of its various hardware opportunities.

III. THE METHOD FOR DETERMINATION OF RESPONSES TO TEST SEQUENCE FOR A NETWORK OF INTERCONNECTIONS

This chapter describes how to find out values of serial vectors that are expected as responses to test sequences for interconnection lines. These vectors may contain errors caused by both static and dynamic faults in interconnections.

The key issue for the method disclosed herein lies in use of the Chinese reminder theorem. One of major areas where that theorem is applied is cryptography [8]. However, in the field of testing that theorem has been applied to engineering of a modular compactor of tests responses and proofing perfect diagnostic properties of it [14]. The option of the Chinese remainder theorem related to polynomials of GF(2) field is provided below [12]:

Theorem 1 (Chinese remainder theorem)

Let us consider a k-component set of remainders $r_i(x)$ obtained from Euclidean division of the $w(x)$ polynomial by the $p_i(x)$ polynomials, where $i = 1,2,\dots,k$, and the set is defined by the following system of congruences:

$$\begin{gathered} w(x) \equiv r_1(x) \left(mod\ p_1(x)\right) \\ w(x) \equiv r_2(x) \left(mod\ p_2(x)\right) \\ \dots \\ w(x) \equiv r_i(x) \left(mod\ p_i(x)\right) \\ \dots \\ w(x) \equiv r_k(x) \left(mod\ p_k(x)\right) \end{gathered} \tag{1}$$

Let us also assume that any two polynomials $p_i(x)$ and $p_j(x)$ are pairwise coprime, i.e. decomposition results for these polynomials into prime factors contain no common factors. In other words, the greatest common divisor $GCD\left(p_i(x), p_j(x)\right) = 1$ for $i,j = 1,2,\dots,k$ and $i \neq j$, where $GCD\left(p_i(x), p_j(x)\right)$ stands for the greatest common divisor of $p_i(x)$ and $p_j(x)$ polynomials. The common solution $w(x)$ for the system of congruences (1) exists and each two solutions are congruent to one another modulo $P(x)$, where:

$$P(x) = \prod_{j=1}^{k} p_j(x) \tag{2}$$

Proof:

The complete proof of the foregoing theorem can be found in [8]. Below only the way for determination of the $w(x)$ polynomial is shown. ♦

To find out the form of the $w(x)$ polynomial it is first necessary to calculate values of the following polynomials:

$$P_i(x) = \prod_{j=1, j\neq i}^{k} p_j(x) \tag{3}$$

For $i = 1,2,\dots,k$ the $p_i(x)$ and $P_i(x)$ polynomials are pairwise coprime, i.e. they have no common dividers except for unity.

$$GCD\left(p_i(x), P_i(x)\right) = 1 \tag{4}$$

Therefore there always exists such a polynomial $Q_i(x)$ that meets the following congruence:

$$P_i(x) \cdot Q_i(x) \equiv 1 \left(mod\ p_i(x)\right) \tag{5}$$

The value of the $Q_i(x)$ polynomial can be found out from the foregoing relationship by means of the Euclidean algorithm [18, 19]. Finally, the value of the $w(x)$ polynomial is defined by the following equation:

$$w(x) = \sum_{i=1}^{k} \oplus [r_i(x) \cdot P_i(x) \cdot Q_i(x)] \ mod\ P(x) \qquad (6)$$

In practice, the $w(x)$ polynomial mentioned in Theorem 1 corresponds to a sequence $\boldsymbol{w}$ that is a response to the test sequence delivered to the interconnection in question. The sequence is supplied to the U_0 input of a MISR register with programmable feedback. Later on that register shall be also designated with the PMISR acronym (*Multi-Input Signature Register with Programmable linear feedback*). The general schematic diagram of such an *n*-bit register is shown in Fig. 3. The $p_{i,0}, p_{i,1}, \ldots, p_{i,n-1}, p_{i,n}$ coefficients of the $p_i(x)$ polynomial define feedback configuration for the PMISR register whilst the $a_0, a_1, \ldots, a_{n-1}$ can be used to select the register input where the $\boldsymbol{w}$ sequence already received from the interconnection under test is supplied. Should the $\boldsymbol{w}$ is to be supplied to the U_o input of the register the foregoing parameters must adopt the following values: $a_0 = 1$ and $a_1 = = a_2 = \cdots = a_{n-1} = 0$.

Determination of k remainders denominated as $r_i(x)$ in Theorem 1 need k analyzes (compaction operations) of the $\boldsymbol{w}$ sequence to be carried out by means of the PMISR register. For each i^{th} analysis the register must be properly configured so that its linear feedback can be defined by the $p_i(x)$ polynomial. Each i^{th} analysis results in the $s_{i,0}(x)$ signature that remains in the PMISR register and can be converted into the $r_i(x)$ remainder. However, in case of the PMISR register from Fig. 3, the remainder equals to the signature, tj. $r_i(x) = = s_{i,0}(x)$. The notation $s_{i,j}(x)$ stands here for the polynomial that corresponds to the signature obtained as a result from the i^{th} analysis of the $\boldsymbol{w}$ sequence delivered to the j^{th} input of the MISR register. The way how to convert the $s_{i,j}(x)$ signature into the $r_i(x)$ remainder for $j = 1,2, \ldots, n\text{-}1$ shall be explained in a further part of this chapter.

Below are some important conclusions about the proposed method of determining the test response sequence based on the set of signatures [12].

Conclusion 1

The values of $P_i(x)$, $Q_i(x)$ and $P(x)$ polynomials depend exclusively on the $p_i(x)$ polynomials that define the feedback of the MISR register during k subsequent analyzes of the $\boldsymbol{w}$ sequence $(i = 1,2, \ldots, k)$ but are independent on the $w(x)$ polynomial associated with the mentioned sequence. Thus, the $P_i(x)$, $Q_i(x)$ and $P(x)$ polynomials can be determined only once and then these polynomials can be repeatedly used to find out various $\boldsymbol{w}$ sequences. ♦

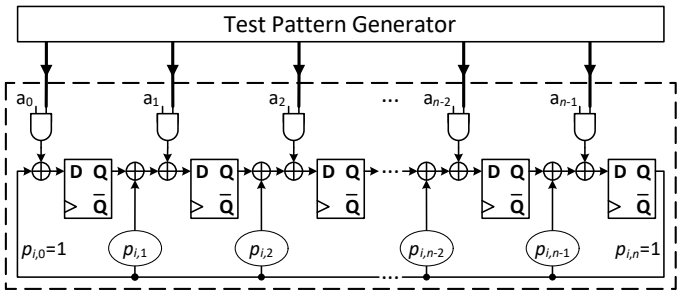

Fig. 3. Schematic diagram of an *n*-bit MISR with programmable linear feedback; the MISR is designed to compact test responses received from a network of interconnections

Conclusion 2

When $\deg(w(x)) < \deg(P(x))$ the set of congruences (1) has only one solution. In other words, there is only one $w(x)$ polynomial that matches the set of congruences (1). ♦

Conclusion 3

Let us assume that an *n*-bit MISR register is used for analysis of the $\boldsymbol{w}$ sequence with the length of m. Therefore, $\deg(w(x)) < m$ and $\deg(p_i(x)) = n$ for $i = 1,2, \ldots, k$. To find out the value of the $w(x)$ polynomial in unambiguous way it is necessary to calculate $k = \lceil m/n \rceil$ number of $r_i(x)$ remainders obtained from division of the $w(x)$ polynomial by k various $p_i(x)$ polynomials, where $i = 1,2, \ldots, k$. Nevertheless, the $p_i(x)$ polynomials must meet mandatory conditions set forth in Theorem 1. ♦

Conclusion 4

To improve reliability and trustworthiness of the method presented herein one has to carry out an additional, the $(k+1)^{th}$ analysis of the $\boldsymbol{w}$ sequence. Should all values of that sequence calculated on grounds of all k-component subsets of the $(k+1)$-component set of signatures are identical the identification process of the $\boldsymbol{w}$ sequence was carried out with no errors. ♦

Example 2

The binary sequence $\boldsymbol{w}$ with the length of $m = 15$ bits and with the unknown content was three times delivered to the U_o input of the MISR register with the length of $n = 5$ bits. The experiments employed the MISR register with programmable feedback and with $k = 3$ possible different configurations defined by the following polynomials:

$$p_1(x) = x^5 + x^2 + 1,$$
$$p_2(x) = x^5 + x^3 + x^2 + x + 1,$$
$$p_3(x) = x^5 + x^4 + x^2 + x + 1.$$

The three subsequent experiments carried out with the $\boldsymbol{w}$ sequence have led to the following signatures: $\boldsymbol{s_1} = \langle 10111 \rangle$, $\boldsymbol{s_2} = \langle 00011 \rangle$, $\boldsymbol{s_3} = \langle 01111 \rangle$, where each of the $\boldsymbol{s_i}$ signatures was obtained by means of the MISR register with the feedback defined by the respective $p_i(x)$ polynomial, where $i = 1,2,3$. Since the experiments were carried out with use of the IED-MISR register the following relationship takes place: $r_i(x) = s_i(x) \mathrel{\hat{=}} \boldsymbol{s_i}$. The set of three remainders corresponding to $\boldsymbol{s_1}$, $\boldsymbol{s_2}$ and $\boldsymbol{s_3}$ signatures is disclosed below:

$$r_1(x) = x^4 + x^2 + x + 1,$$
$$r_2(x) = x + 1,$$
$$r_3(x) = x^3 + x^2 + x + 1.$$

To find out formulation for the $w(x)$ polynomial corresponding to the $\boldsymbol{w}$ sequence to be found the (6) equation was used. For that purpose it was first necessary to establish forms of $P_i(x)$, $Q_i(x)$ and $P(x)$ polynomials for $i = 1,2,3$.

$$P_1(x) = x^{10} + x^9 + x^8 + x^7 + x^6 + x^4 + x^3 + x^2 + x + 1$$
$$P_2(x) = x^{10} + x^9 + x^3 + x + 1$$
$$P_3(x) = x^{10} + x^8 + x^6 + x^5 + x^4 + x + 1$$
$$Q_1(x) = x^4 + x^2 + x + 1$$

$$Q_2(x) = x^4 + x^3 + x^2 + 1$$
$$Q_3(x) = x^3 + x + 1$$
$$P(x) = x^{15} + x^{14} + x^{13} + x^9 + x^8 + x^3 + 1$$

The $w(x)$ polynomial together with the corresponding $\boldsymbol{w}$ sequence is provided below:

$$w(x) = x^{14} + x^{13} + x^{11} + x^8 + x^5 + x^4 + x^3 + 1$$
$$\mathbf{w} = \langle 110100100111001 \rangle \quad \blacklozenge$$

Example 3

The $\boldsymbol{T}$ sequence from Table II was six times delivered by the test pattern generator to the input of a faulty interconnection. The interconnection output is connected to the U_o input of the MISR register from Example 2. By proceeding in a similar manner as shown in Example 2, a set of six signatures was obtained. These signatures together with the algorithm associated with Theorem 1 were used to find out the content of the $\boldsymbol{R}$ sequence being the response of the investigated interconnection to the test. The sequence is provided in the second row of Table II.

The comparison between the $\boldsymbol{T}$ and $\boldsymbol{R}$ sequences makes it possible to conclude that the propagation delay respectively for raising and falling edges equal to $t_r = 2$ and $t_f = 1$ clock periods of the synchronization frequency for the MISR register. In turn, a short negative pulse appearing in the output signal from the interconnection under test, manifested as a single '1' in the $\boldsymbol{R}$ sequence (highlighted with white color on gray background in Table II) can be an effect of crosstalks between interconnections. Detailed interpretation of obtained results shall depend on the circuit topology and specific properties of the network of connections under test. ♦

The foregoing Example 2 explains how to find out the $\boldsymbol{w}$ sequence delivered to the U_0 input of the MISR register. However, the question arises how to find out the content of $\boldsymbol{w}$ sequence delivered to one of other U_j inputs of the MISR register, where $j = 1,2,\dots,n-1$. The question can be answered by Property 1.

Property 1

Let us assume that the $\boldsymbol{w}$ sequence is delivered to the U_j input of the MISR register as shown in Fig. 3, where $j = 0,1,2,\dots,n-1$. Let us also use the $r_{i,j}(x)$ designation as the remainder from division of the $w(x)$ polynomial corresponding to the $\boldsymbol{w}$ sequence by the $p_i(x)$ polynomial representing the i^{th} configuration of the linear feedback for the mentioned MISR register. If so, $r_{i,0}(x) = r_i(x)$, where $r_i(x)$ stands for the remainder that was used for the i^{th} congruence of Theorem 1. Other $r_{i,j}(x)$ remainders can be derived from the $r_{i,0}(x)$ remainder owing to the following relation [11, 12]:

$$r_{i,j}(x) = x^j \cdot r_{i,0}(x) \; mod \; p_i(x) \tag{7}$$

Thus, the following equation is correct as well:

$$r_{i,j}(x) = x^j \cdot r_i(x) \; mod \; p_i(x) \tag{8}$$

If the $p_i(x)$ polynomial in the foregoing equation (8) is a prime polynomial, the $p_i(x)$ and x^j are pairwise coprime, i.e. have no common dividers except for the unit.

$$GCD(p_i(x), x^j) = 1 \tag{9}$$

Therefore there is always such a $z_{i,j}(x)$ polynomial that meets the following congruence:

$$x^j \cdot z_{i,j}(x) \equiv 1 \left(mod \; p_i(x)\right) \tag{10}$$

The $z_{i,j}(x)$ polynomial can be found out by means of the Euclidean algorithm [18, 19]. Then the $r_i(x)$ remainder can be established with use of the formula below:

$$r_i(x) = z_{i,j}(x) \cdot r_{i,j}(x) \; mod \; p_i(x) \tag{11}$$

where $j = 0,1,2,\dots,n-1$. ♦

TABLE II
The sequence $\boldsymbol{S}$ of the test input and the sequence $\boldsymbol{R}$ of the test response for the interconnection under test

T:	00000011111100000011111100000011111
R:	00000000111110000100011111000000001111

Example 4

Let us assume that the $\boldsymbol{w}$ polynomial has been three times supplied to the U_1 input of the MISR register from Example 3 and the following set of signatures was obtained: $\boldsymbol{s_{1,1}} = \langle 01011 \rangle$, $\boldsymbol{s_{2,1}} = \langle 00110 \rangle$, $\boldsymbol{s_{3,1}} = \langle 11110 \rangle$. The respective remainders corresponding to individual signatures are

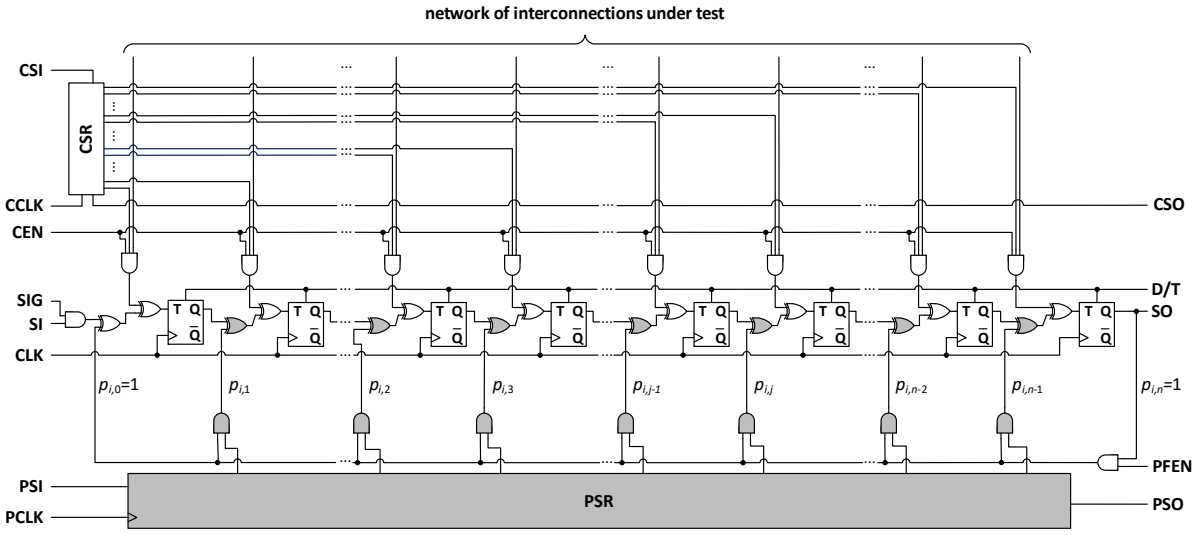

Fig. 4. Scheme of the PCOMP module

$r_{1,1}(x) = x^3 + x + 1$, $r_{2,1}(x) = x^2 + x$, $r_{3,1}(x) = x^4 + x^3 + x^2 + x$. These remainders should serve as a baseline to find out a set of three remainders $r_1(x)$, $r_2(x)$, $r_3(x)$ that would be recorded if the $\boldsymbol{w}$ sequence was supplied to the U_0 input of the MISR register. For that purpose the Property 1 shall be used but it is first necessary to establish the $z_{i,j}(x)$ polynomials, where $j = 1$ and $i = 1, 2, 3$. These polynomials are summarized below:

$$z_{1,1}(x) = x^4 + x,$$
$$z_{2,1}(x) = x^4 + x^2 + x + 1,$$
$$z_{3,1}(x) = x^4 + x^3 + x^2 + 1.$$

Then, based on the equation (11) the following solution of the foregoing problem can be obtained:

$$r_1(x) = z_{1,1}(x) \cdot r_{1,1}(x) \; mod \; p_1(x) = x^4 + x^3 + x + 1,$$
$$r_2(x) = z_{2,1}(x) \cdot r_{2,1}(x) \; mod \; p_2(x) = x + 1,$$
$$r_3(x) = z_{3,1}(x) \cdot r_{3,1}(x) \; mod \; p_3(x) = x^3 + x^2 + x + 1.$$

Please note that the remainders $r_1(x)$, $r_2(x)$ and $r_3(x)$ obtained for this example are exactly the same as the ones from Example 2. ♦

IV. HARDWARE IMPLEMENTATION OF THE METHOD

The hardware of the method disclosed above and developed to determine sequences of test responses is based on the IBIST architecture, which was presented in [11]. The extended form of an n-bit COMP module revealed in the aforementioned study is shown in Fig. 4. The supplementary components that were added are limited merely to the $(n\text{-}1)$-bit shift register PSR, n-1 XOR gates and n-1 two-input AND gates. All these components are highlighted in the figure in grey. Such a modified COMP module shall be denoted with the acronym PCOMP. Prior to execution of tests the PSR register is uploaded with the configuration vector for the linear feedback of the PMISR register, where the vector is serially shifted from an external tester. Output signals of the PSR register correspond to coefficients of the $p_i(x)$ polynomial that defines the feedback loop, which is indicated in the figure.

The block schematic of the IBIST structure capable of supporting detection and identification of both static and dynamic faults in interconnection networks is shown in Fig. 5. Only the module designated with 'B' is of the PCOMP type whilst all modules with numbers from 1 to B-1 are of the COMP type. Such an IBIST structure enables that at any specific moment of time a test response vector received from only a single, discretionally selected interconnection is recorded. Hence, when investigation of test response sequences for a large number faulty interconnections is a point it needs relatively long testing time. On the other hand, the IBIST structure as above brings in only an insignificant hardware redundancy. Hereinafter the hardware redundancy shall be related to the IBIST structure disclosed in [11] and shown in Fig. 1.

For needs related to detection and identification of dynamic faults in selected interconnections of the network all COMP modules must be arranged in such a way that MISR registers contained in each module can perform as a single MIShR register with the total length of $(B\text{-}1) \cdot n$ bits. For that purposes it is necessary to utilize an additional signal called MEN (*MIShR Enable*) designed to control the SIG input of $COMP_1$ module whilst all SIG inputs of other COMP modules as well as the PCOMP module shall be controlled by the common SIG line. The PCOMP module should operate as a PMISR register with the serial input (SI) connected to the serial output (SO) of the MIShR register (the SO output of the $COMP_{B\text{-}1}$ serves as the serial output of the entire MIShR register). To have the COMP and PCOMP modules arranged in the foregoing way the control signals must adopt the following levels: CEN = 1, FEN = 0, PFEN = 1, SIG = 1, MEN = 0 and D/T = 0. In addition, all MISR registers of COMP modules as well as the PMISR register of the PCOMP module must be cleared prior to each collection procedure of the test response sequence.

Let us assume that the faulty line to be tested for determination of the test response sequence is connected to the j^{th} input of the l^{th} COMP module, where $j = 0,1, \ldots, n\text{-}1$ and $l = 1,2, \ldots, B\text{-}1$. The interconnection assigned for testing is selected by loading appropriate masking vectors into CSR registers of all COMP modules as well as the PCOMP module.

The CSR register of the $COMP_l$ module must be loaded

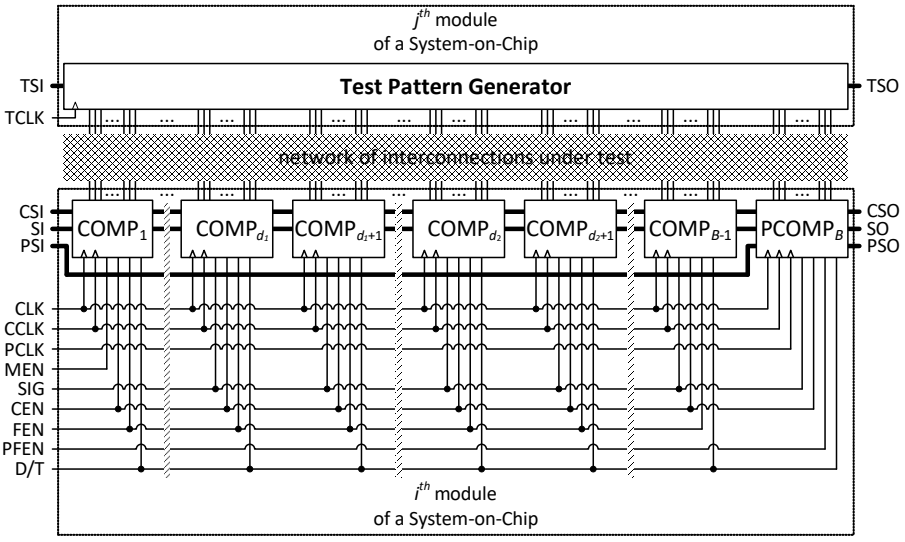

Fig. 5. Block diagram of the IBIST structure comprising a single module of the PCOMP type

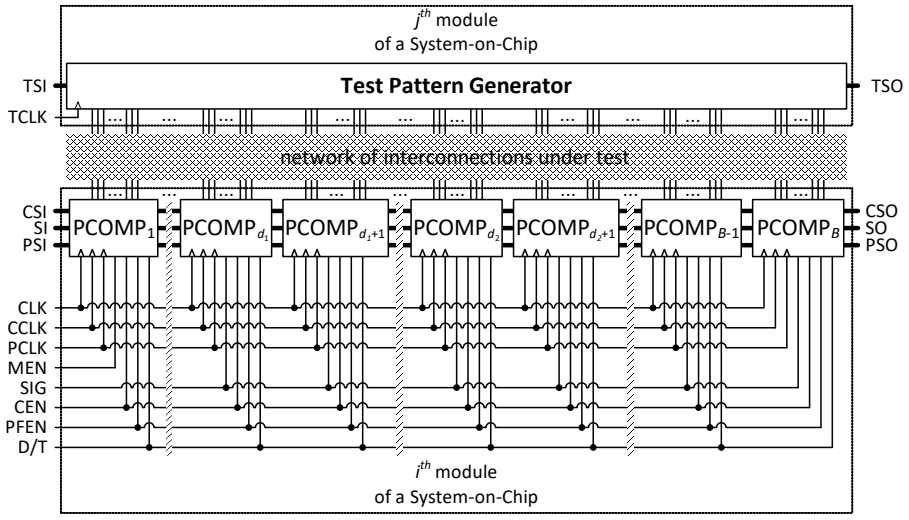

Fig. 6. Block diagram of the IBIST structure made exclusively of the PCOMP-type modules

with the masking vector where only the bit number j adopts the high level ('1') level and all other bits are low ('0'). Simultaneously, the CSR registers of all other COMP modules as well as the PCOMP module must be cleared (zeroed). After such preparation of COMP modules the aforementioned MIShR register shall practically perform as a shift register with the length of ρ and to deliver the vector of test response received from the interconnection under test shall be delivered to the SI input of the PMISR register incorporated into the PCOMP module. The length ρ of the shift register shall be expressed by means of the following formula:

$$\rho = [(B-1)-l]\cdot n + (n-j) = (B-l)\cdot n - j \qquad (12)$$

where $l = 1,2,\ldots,B\text{-}1$ and $j = 0,1,\ldots,n\text{-}1$.

The PCOMP module can be also used for compaction of test response sequences for interconnection lines delivered to parallel inputs of the module. The interconnection to be tested can be selected in the same way as in case of the aforementioned COMP$_l$ module, i.e. by loading the CSR register of the PCOMP module with the appropriate masking vector. Moreover, the control signals should adopt the following levels: CEN = 1, PFEN = 1, SIG = 0, D/T = 0 whilst the levels of the FEN and MEN signals are irrelevant.

Determination of the $\boldsymbol{w}$ sequence of test response for the interconnection line delivered to one of the PCOMP module needs k-fold repetition of the test sequence delivery to the inputs of the interconnection network and to take k recording of the test response, where $k = \left\lceil \frac{m}{n} \right\rceil$.

The foregoing operation produces k various signatures that correspond to the $\boldsymbol{w}$ sequence. But when lines under test are connected to parallel inputs of COMP modules the IBIST structure from Fig. 5 makes it possible to reduce the number of signatures that have to be determined by means of the PCOMP module. Let us remind once again that the test is carried out for the j^{th} input of the COMP$_l$ module. Such a test needs compaction of m-ρ bits in the $\boldsymbol{w}$ sequence to be executed for each collection of the $\boldsymbol{w}$ sequence received as a test response for the specific interconnection line. The remaining ρ bits of the response sequence kept in the MIShR register made up of COMP modules can be evacuated only once and delivered directly to an external tester together with the first signature formed by the PCOMP module. Thus, the number of

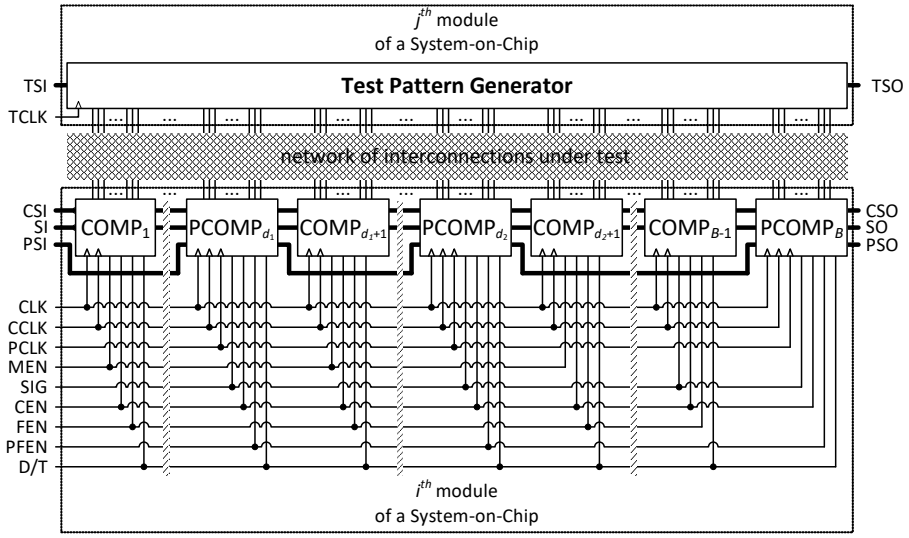

Fig. 7. Block diagram of the IBIST structure comprising D = 3 modules of the PCOMP type

compaction operations necessary to find the $\boldsymbol{w}$ sequence as well as the number of signatures that have to be determined by means of the PCOMP module shall be reduced to the number of $k' = K(\rho) = \lceil (m-\rho)/n \rceil$, where $k' \leq k$.

Another implementation of the IBIST capable of supporting detection and localization of both static and dynamic faults in interconnection lines is shown in Fig. 6. Herein all modules are of the PCOMP type.

Such a structure enables simultaneous analysis of sequences received from not more than B faulty interconnection lines provided that each interconnection line is connected to one of parallel inputs within a different PCOMP module. It is the advantage that enables substantial reduction of time that is necessary for detection and localization of dynamic faults in interconnections. However, drawback of the solution disclosed in Fig. 6 consists in substantial redundancy of hardware that is B times higher than in case of the IBIST structure from Fig. 5.

The balance between time that is necessary for diagnostics of dynamic faults affecting interconnection lines and hardware redundancy carried in by the IBIST structure can be achieved when only selected COMP modules from Fig. 1 are substituted with PCOMP modules. An example of such a IBIST structure with three modules PCOMP_{d1}, PCOMP_{d2} and PCOMP_B is shown in Fig. 7. Please pay attention that the set of $\{\text{COMP}_f\}$ modules together with the PCOMP_{d1} module, where $f = 1, 2, \ldots, (d_1 - 1)$ is a solution that is very similar to the one from Fig. 5. The same refers to the set of $\{\text{COMP}_g\}$ together with the PCOMP_{d2} module, also $\{\text{COMP}_h\}$ modules and the PCOMP_{d2} module as well as the set of $\{\text{COMP}_h\}$ module and the PCOMP_B module, where $g = (d_1 + 1), (d_1 + 2), \ldots, (d_2 - 1)$ and $h = (d_2 + 1), (d_2 + 2), \ldots, (B - 1)$. Therefore the IBIST structure as shown is Fig. 7 enables simultaneous analysis of sequences received as responses from tests of three separate interconnections. To enable parallel operation of the foregoing fragments associated with the three aforementioned PCOMP_{d1}, PCOMP_{d2} and PCOMP_B modules, the SIG inputs of the COMP_1, $\text{COMP}_{(d1+1)}$ and $\text{COMP}_{(d2+1)}$ modules must be controlled by the common signal MEN.

In general, the IBIST structure from Fig. 7 may comprise D modules of PCOMP type, where $1 \leq D \leq B$. Nevetheless, two specific cases, i.e. for $D = 1$ and $D = B$, lead to circuits that are shown in respective drawings in Fig. 5 and he recommended location of the PCOMP modules in the IBIST structure in question is defined by Observation 1.

Observation 1

To reduce the total time that is necessary to determine binary sequences recorded as responses to tests for all interconnections within the network under test, the PCOMP_{d_x} modules must be deployed in the IBIST structure in a specific manner so that their indexes d_x meet the following relationships:

$$D|B \Longrightarrow \left(d_x = x \cdot \frac{B}{D} \;\; for \; x = 1,2,\ldots,D\right) \tag{13a}$$

$$D \dagger B \Longrightarrow d_x = \begin{cases} x \cdot \left\lfloor \frac{B}{D} \right\rfloor & for \quad x = 1,2,\ldots,Z \\ (x - Z) \cdot \left\lfloor \frac{B}{D} \right\rfloor + Z \cdot \left\lfloor \frac{B}{D} \right\rfloor & for \quad x = Z+1,\ldots,D \end{cases} \tag{13b}$$

where: $Z = D \cdot \left\lfloor \frac{B}{D} \right\rfloor - B$. ♦

Meeting of the foregoing requirements leads to the IBIST structure where the number of COMP modules associated with each of the PCOMP modules are the same or at least similar.

Example 5

Let us assume that the total number of both COMP and PCOMP modules incorporated into the IBIST structure as shown in Fig. 7 is $B = 19$. The number of PCOMP modules within that structure is $D = 3$ and one of these modules is indexed as $B = 19$. Indexes d_1 and d_2 of the remaining two modules can be determined pursuant to instructions entailed by Observation 1. Since B is indivisible (without a remainder) by D $(i.e. D \dagger B)$, the equation (13b) can be applied. First the value of Z is calculated, where $Z = D \cdot \left\lfloor \frac{B}{D} \right\rfloor - B = 3 \cdot \left\lfloor \frac{19}{3} \right\rfloor - 19 = 2$. Hence, the values of d_1 and d_2 can be calculated from equation (13b): $d_1 = 1 \cdot \left\lfloor \frac{19}{3} \right\rfloor = 6$, $d_2 = 2 \cdot \left\lfloor \frac{19}{3} \right\rfloor = 12$. One can also notice that the index d_3 of the third PCOMP module can be calculated from equation (13b) and is found as $d_3 = (3-2) \cdot \left\lfloor \frac{19}{3} \right\rfloor + 2 \cdot \left\lfloor \frac{19}{3} \right\rfloor = 19 = B$. ♦

The essential property of the solution disclosed in this study is the total time τ_{diag} needed for diagnostics of the interconnection under test and necessary to establish a response sequence to the test. That time is a superposition of two components: $\tau_{diag} = \tau_{test} + \tau_{scan}$. The symbol τ_{test} stands for the time that is necessary to deliver a test sequence to inputs of an interconnection network, whilst τ_{scan} is the time necessary for initiation of the test pattern generator and PCOMP modules as well as for serial shifting of resulting signatures into an external tester. Let us assume that the input sequence is delivered to inputs of interconnections with the frequency of f_{test} and serial communication with an external tester is clocked by the frequency denoted as f_{scan}, where the f_{test} frequency is much higher than the f_{scan} frequency, i.e. $\frac{f_{test}}{f_{scan}} = \gamma \gg 1$. For simplicity of the analysis the parameter τ_{diag} neglects the time that is necessary for the external tester for calculations that are needed to find out the response sequence to the test for the investigated interconnection on grounds of collected signatures. Let us also assume that the number v of interconnections within the network is divisible by length n of COMP and PCOMP modules , i.e. $v = B \cdot n$.

Now, let us consider a BIST structure that is analogous to the one as shown in Fig. 7. Such a structure shall comprise D modules of PCOMP type deployed according to the rules established in Observation 1. The most time-consuming operation is determination of the test response sequence when interconnections under tests are connected to parallel inputs of the PCOMP modules. The formulas that enable calculation of

the maximum time τ_{diag} for one of such interconnections are provided below:

$$\tau_{diag\_max} = \tau_{test\_max} + \tau_{scan\_max} \tag{14}$$

where:

$$\tau_{test\_max} = \frac{k \cdot m}{f_{test}} = \frac{\left\lceil \frac{m}{n} \right\rceil \cdot m}{f_{test}} \tag{15}$$

and

$$\tau_{scan\_max} = \frac{v + k \cdot B \cdot n}{f_{scan}} = \frac{B \cdot n \cdot \left(\left\lceil \frac{m}{n} \right\rceil + 1 \right)}{f_{scan}} \tag{16}$$

The parameter designated as τ_{test_max} stands for the time that is necessary for the PMISR register incorporated into the PCOMP_{d1} module to carry out k number of compaction operations of the $\boldsymbol{w}$ sequence collected as a test response for the interconnection under test, where the $\boldsymbol{w}$ sequence counts m bits. The mentioned parameter τ_{scan_max} has two components. One of them is the time that is needed for serial shifting of initial seeding from an external tester into the test pattern generator prior to the first measurement (compaction). It is the operation that takes $v = B \cdot n$ of clock pulses. The second component corresponds to the time that is necessary for serial evacuation of signatures obtained from k compactions and shifting them into an external tester. Such an operation takes $k \cdot B \cdot n$ clock pulses.

To estimate the total time that is needed to detect and localize dynamic faults for more interconnections it is convenient to know the average time τ_{diag_avr} necessary to establish a sequence of test response for a single interconnection. Such a time period is defined as a quotient of the total time needed to establish sequences of test responses for all interconnections within the network over the number v of such interconnections.

$$\tau_{scan\_avr} = \tau_{test\_avr} + \tau_{scan\_avr} \tag{17}$$

where time parameters τ_{test_avr} and τ_{scan_avr} are defined by means of the following equations:

$$\tau_{test\_avr} = \frac{L \cdot m}{v \cdot f_{test}} \tag{18}$$

$$\tau_{scan\_avr} = \frac{v + L \cdot B \cdot n}{v \cdot f_{scan}} = \frac{L + 1}{f_{scan}} \tag{19}$$

The L parameter in the foregoing equations stands for the total number of compaction operations for test response sequences for all interconnections within the network.

$$L = \sum_{\rho=1}^{\left(\left\lceil \frac{B}{D} \right\rceil - 1\right) \cdot n} K(\rho) + k \cdot n = \sum_{\rho=1}^{\left(\left\lceil \frac{B}{D} \right\rceil - 1\right) \cdot n} \left\lceil \frac{m - \rho}{n} \right\rceil + \left\lceil \frac{m}{n} \right\rceil \cdot n \tag{20}$$

The time parameters τ_{diag_max} and $\tau_{diag_{avr}}$ were calculated for networks of interconnections with four various numbers of lines, i.e. $v \in \{1024, 2048, 4096, 8192\}$ and summarized in Table III. The network under test was stimulated by means of the MAFM test sequence containing $m = 6 * v$ vectors. It was assumed that the length of each COMP and PCOMP module was $n = 32$, which is the recommended size due to fault aliasing. The total number of both COMP and PCOMP modules embedded into the IBIST structure for each network of interconnections was calculated as $B = \left\lceil \frac{v}{n} \right\rceil$, therefore $B \in \{32, 64, 128, 256\}$. The calculations were completed for various number (D) of PCOMP modules in the IBIST structure, where $D \in \{1,2,4,8,16,32,64,128,256\}$ and $D \leq B$. It was also assumed that the test sequence is delivered to inputs of the interconnection network at the frequency of $f_{test} = 1$ GHz whilst serial communication with an external tester is clocked with the frequency of $f_{scan} = = 100$ MHz. The table column headed with $\tau_{diag\_20\%}$ summarizes maximum and average times that are necessary to establish sequences of test responses for 20% of the network of interconnections (the columns with the respective headers max and avr). The assumption that 20% is the upper limit for the number of interconnections that may suffer faults seems to be justified in the context of information sourced from such studies as [3, 9, 10] where the number of faulty interconnection assumed by authors ranges from 1 to 15%.

TABLE III
MAXIMUM AND AVERAGE TIMES FOR DIAGNOSTICS OF INTERCONNECTIONS FOR $f_{scan} = 100$MHz

v	m	B	D	τ_{diag_max} [ms]	τ_{diag_avr} [ms]	$\tau_{diag\_20\%}$ [s]	
						max	avr
1024	6144	32	1	3.156	2.907	0.65	0.60
			2		1.519		0.31
			4		0.776		0.16
			8		0.392		0.08
			16		0.197		0.04
			32		0.098		0.02
2048	12288	64	1	12.603	11.582	5.17	4.75
			2		6.053		2.48
			4		3.092		1.27
			8		1.562		0.64
			16		0.785		0.32
			32		0.393		0.16
			64		0.197		0.08
4096	24576	128	1	50.373	46.233	41.31	37.91
			2		24.165		19.82
			4		12.344		10.12
			8		6.237		5.11
			16		3.135		2.57
			32		1.571		1.29
			64		0.786		0.64
			128		0.393		0.32
8192	49152	256	1	201.409	184.741	330.11	302.79
			2		96.565		158.27
			4		49.331		80.85
			8		24.927		40.86
			16		12.529		20.53
			32		6.281		10.29
			64		3.144		5.15
			128		1.573		2.58
			256		0.786		1.29

The analysis of data summarized in Table III leads to some observations that include relationships between the times designated as τ_{diag_max} and τ_{diag_avr}, the number v of interconnections in the network under test and the number D of PCOMP modules that are incorporated into the IBIST structure.

Observation 2

When the number of interconnections in the network under test increases twice the both time parameters τ_{diag_max} and τ_{diag_avr} are fourfold higher. The testing time extension is also caused by much longer test sequences since test sequence

TABLE IV
MINIMUM AND MAXIMUM TIMES FOR DIAGNOSTICS OF INTERCONNECTIONS FOR $f_{scan} = 200$MHz

v	m	B	D	τ_{diag_max} [ms]	τ_{diag_avr} [s]	$\tau_{diag\_20\%}$ [s]	
						max	*avr*
1024	6144	32	1	0.00181	2.05	0.444	0.410
			2	0.00199	1.07		0.214
			4	0.00208	0.55		0.109
			8	0.00213	0.28		0.055
			16	0.00215	0.14		0.028
			32	0.00216	0.07		0.014
2048	12288	64	1	0.00723	16.31	3.551	3.265
			2	0.00795	8.52		1.706
			4	0.00831	4.35		0.871
			8	0.00849	2.20		0.440
			16	0.00858	1.11		0.221
			32	0.00863	0.55		0.111
			64	0.00865	0.28		0.055
4096	24576	128	1	0.02888	130.19	28.391	26.064
			2	0.03176	68.05		13.623
			4	0.03321	34.76		6.959
			8	0.03393	17.56		3.516
			16	0.03429	8.83		1.767
			32	0.03447	4.42		0.886
			64	0.03456	2.21		0.443
			128	0.03460	1.11		0.222
8192	49152	256	1	0.11543	1040.46	226.924	208.169
			2	0.12697	543.85		108.810
			4	0.13274	277.83		55.587
			8	0.13562	140.39		28.088
			16	0.13706	70.56		14.118
			32	0.13778	35.37		7.077
			64	0.13814	17.71		3.543
			128	0.13832	8.86		1.772
			256	0.13841	4.43		0.886

length is directly proportional to the number of interconnections. It is why the τ_{diag_max} and τ_{diag_max} time parameters increase fourfold instead of two times. ♦

Observation 3

Twofold growth of the D number of PCOMP-type modules incorporated into the IBIST structure leads to about two times shorter average time necessary to find out a test response for a single interconnection, i.e. τ_{diag_avr} The error of the foregoing approximation never exceeds 5%. ♦

Observation 4

The τ_{diag_max} time is roughly D times longer than the τ_{diag_avr} parameter, i.e. $\tau_{diag\_max} \cong D \cdot \tau_{diag\_avr}$. The approximation error for that case is less or equal 10%. ♦

To investigate how frequency of serial data exchange with the external tester affects the maximum and average time for fault detection the foregoing calculations were repeated for $f_{scan} = 200$ MHz. Results of the investigations are summarized in Table IV. The observation entailed by comparison between contents of Tables III and IV is disclosed herein.

Observation 5

When the frequency f_{scan} for serial data transmission between an external tester and the IBIST structure increases twofold the time parameters, i.e. τ_{diag_max} and τ_{diag_avr} are reduced by 1.5 times. ♦

The longest time of fault diagnostics τ_{diag_max} obtained from calculations was about 330 s = 5.5 min. It is the time that is needed to establish $1639 \cong 8192 \cdot 20\%$ response sequences by means of the IBIST structure disclosed in Fig. 3 and comprising only one PCOMP module to the test sequence made up of $m = 49152$ test vectors delivered to inputs of the network of interconnections under test. The foregoing testing time was obtained for the lower frequency (of the two frequencies considered in this study, i.e. $f_{scan} = 100$ MHz) for serial communication with an external server.

Let us assume that the price for one second operation of an external tester is 1¢ [17]. If so, the price for using an external tester to identify dynamic faults affecting 20% of interconnections within each of the networks under consideration should not exceed USD 5.5. In practice, identification of faults in interconnections between modules of systems on chips is indispensable only for some of such systems. Moreover, the number of faulty interconnections between modules within a single SoC usually fluctuates about several dozen or several hundred rather than several thousand. Hence one can accept that implementation of the method disclosed in this study and dedicated for determination of test response sequences shall only insignificantly affect manufacturing expenses for a whole series of SoCs. One of the methods that may contribute to reduction of the maximum testing time with consequential mitigation of expenses for operation of an external tester consists in increasing the number of the PCOMP modules incorporated into the IBIST structure but is shall be paid off by more extensive hardware surplus.

V. SCENARIOS FOR TESTING AND DIAGNOSTICS OF DYNAMIC FAULTS

This part of the study discloses a scenario for testing and diagnostics of static and dynamic faults that may affect interconnecting lines. The workflow presented herein is developed for the IBIST structure presented in Fig. 5. However, testing and diagnostics of faults in structures shown in Fig. 6 and Fig. 7 shall follow a similar procedure.

An important premise for the testing scenario disclosed in a further part of this study and dedicated to networks of interconnections consists in verification whether the hardware for determination of signatures is in sound operating condition. Such an approach enables high dependability of results obtained from tests [7]. Should any hardware defect is detected the testing process must be immediately interrupted and further time-consuming processes of fault identification with possible reconfiguration of the interconnection network must be abandoned. Further deliberations assume that only one fault of the stuck-at-level type may occur in the entire compactor but any number of faults, both of the stuck-at-level type and shorts may occur in the interconnection network under test.

Subsequent steps of the suggested test scenario are outlined below.

Step 1: testing of CSR and PSR registers as well as D-type flip-flops incorporated into IET-MISR registers

The tests need the following settings of control signals: SIG=1, D/T=0, FEN=0, PFEN=0, CEN=0. If so, the IET-MISR registers are operated in the scan mode during which they serially exchange data with an external tester. First, the serial flush test vector $FT = 00110$ is supplied to the SI input of the $COMP_1$ module. Then the FT vector is followed

with a test vector sequence that is made up of B serial vectors (*feedback test – FBT*), where each vector contains a leading 'one' with subsequent *n-1* nulls, i.e. $FBT = 100 \ldots 0$. At the same time the inverted *FT* vector is delivered to the CSI input of the $COMP_1$ module, i.e. $\overline{FT} = 11001$ and the vector is followed by a string of Bn nulls. In parallel, a test vector $FT^* = 01100$ is shifted to the PSI input of the $PCOMP_B$ module during the last n+4 clock periods with a string of $n-1$ 'ones' followed afterwards. Thus, the total duration of the test is $Bn + 5$ clock periods. If all IET-MISR and CSR registers incorporated into all COMP modules and the PSR register included into the PCOMP module are free of faults the serial vectors FT, $\overline{FT}$ and FT^* should arrive intact to respective SO, CSO and PSO outputs of the $PCOMP_B$ module. The first objective of the foregoing test procedure is to check functioning of D flip flops of all three registers (MISR, CSR and PSR), i.e. to verify whether the flip-flops are capable of performing all four possible transitions between the current and the subsequent state. The test makes it also possible to detect the foregoing faults in feedback loops of T flip-flops embedded into IET-MISR registers (see Fig. 2b): stuck-at-0 in the T node as well as stuck-at-1 in the T, D/T and A nodes. It also detects stuck-at-1 faults at outputs of AND gates connected to parallel outputs of IET-MISR registers. In addition, the *FT* serial test vector detects stuck-at-0 and stuck-at-1 faults at SI inputs as well as SO outputs of all IET-MISR registers. Similarly, the serial test vector $\overline{FT}$ enables detection of stuck-at-0 and stuck-at-1 faults at CSI inputs and CSO outputs of al CSR registers whilst the serial test vector FT^* enables detection of stuck-at-0 and stuck-at-1 faults at the PSI input and PSO output of the PSR register. Moreover, employing of the FT, $\overline{FT}$ and FT^* strings to verify correctness of serial communication with respective IET-MISR, CSR and PSR registers makes it easier to detect possible mutual shorts both between the SI, CSI and PSI inputs as well as the SO, CSO and PSO outputs of these registers. After that test step is completed the flip-flop with the $n-1$ number of each IET-MISR register is set (logic '1' at output) whilst all other flip-flops of these registers are cleared. In addition, all parallel outputs of the CSR registers adopt the low (null) level whilst all parallel outputs of the PSR register within the $PCOMP_B$ module adopt the high (one) level.

Step 2: test of main feedback lines for IET-MISR registers

The next step assumes the following settings for input signals: SIG=0, D/T=1, FEN=1, PFEN=1, CEN=0 and SI=1. It entails operation of IET-MISR registers as independent LFSRs made up of T-type flip-flops. Each of these registers starts is operation cycle from the vector of 10..00, where the leftmost bit is the most significant bit of vector. After a single clock cycle the next step begins where serial data transmission is restored and the content of IET-MISR registers is evacuated and substituted with a string composed of $B \cdot n$ binary ones. The foregoing operation enables detection of stuck-at-0 faults in main feedback loops of IET-MISR registers as well as stuck-at-1 faults in the SIG strobing lines for AND gates at serial inputs (SI) for these registers. If the IET-MISR register reveals no fault it should move to the state that follows the *FBT* state on the graph of the register operation (in case of the IET-MISR register incorporated into the $PCOMP_B$ module that target state is a vector made up exclusively of logic ones). Occurrence of any of the foregoing faults shall lead to a different target state. To complete this step of the test scenario a string made up of n-1 nulls is shifted into the $PCOMP_B$ module.

Step 3: verification of operational soundness of T-type flip-flops

The following settings for control signals: SIG=1, D/T=1, FEN=0, PFEN=0 and CEN=0, make all IET-MISR registers to operate as a single long register made up of T-type flip-flops. The test takes three clock periods and consists in supplying of the '100' string (beginning with '1' and with two subsequent nulls) as a serial vector to the SI input of the $COMP_1$ module. The same string should appear at the output of each defect-free T-type flip-flop as well as the SO output of the $PCOMP_B$ module. The same procedure should clear (set to null) all defect-free T-type flip-flops. It is the test that detects these faults in feedback lines of T-type flip-flops that have not been tested during the first step, i.e. stuck-at-0 and stuck-at-1 at those inputs of AND gates that are connected to Q outputs of D flip-flops as well as stuck-at-0 faults for the D/T signal in Fig. 2b. It also enables detection of stuck-at-1 faults at outputs of the PSR register. The next step assumes setting of control signals FEN=1 and PFEN=1 to enable activation of main feedback lines of the IET-MISR registers for one clock period. Defect-free IET-MISR registers should preserve all-null content, which confirms lack of stuck-at-1 faults in main feedback loops of these registers. The foregoing test outcome is verified by serial evacuation of the register content with refilling all IET-MISR registers in all COMP modules with zeros and shifting the *FTB* string into the IET-MISR register of the PCOMP module. At the same time the test pattern generator is loaded with an all-ones vector and the PFEN signal is set (PFEN=1) for one clock period. Next, the serial input of the $COMP_1$ module is cleared (SI=0) and the content of the IET-MISR register incorporated into the $PCOMP_B$ module is evacuated to an external tester during subsequent n clock periods. If no stuck-at-1 faults occur at parallel outputs of the PSR register the string evacuated from the aforementioned IET-MISR register should be 00...01 (i.e. a binary '1' should occur exclusively at the least significant position). That step of the test scenario is completed by serial shifting of a sequence corresponding to the $p_T(x)$ polynomial into the PSR register of the $PCOMP_B$ module. Hence the subsequent step of the test scenario begins with exactly the same feedback loops of IET-MISR registers in all modules.

Step 4: test of AND gates connected to parallel inputs of the IET-MISR registers

Since stuck-at-0 faults at inputs and outputs of each three-input AND gates connected to inputs of the IET-MISR registers are indistinguishable from stuck-at-0 faults affecting the interconnection under test, such faults can be detected during the phase of fault localization. Also stuck-at-1 faults at the interconnection under test shall be detected during the same phase. During the current phase of tests it is enough to detect stuck-at-1 at inputs of each AND gate connected to outputs of the CSR register and to the CEN line. To accomplish it the inputs in question must be stimulated with corresponding vectors 01 and 10. For that purpose the control signals should adopt the following levels: SIG=1, D/T=1,

FEN=1, PFEN=1, SI=0 and CEN=0. Then the CEN signal is switched to '1' for one clock period to enable supplying of the 01 vector to respective inputs of each AND gate (by the end of step 1 all outputs of the CSR registers were cleared to logic '0' /null). Then the CSR registers should be filled with the string of $B \cdot n$ binary ones ('1'). Upon completion of the latter respective inputs of each gate are stimulated with the '10' vector (the CEN line readopts the CEN=0 level). If none AND gate at parallel inputs of the IET-MISR registers is defective all these registers are successfully cleared. It can be checked after having evacuated content of all IET-MISR registers into an external tester with simultaneous shifting all-zero strings into the registers. At the same time the test pattern generator is serially loaded with an initial vector of the test sequence designed to detect faults in the network of interconnections.

Step 5: detection of faults in the network of interconnections

Let us set the control signals in the following way: SIG=0, D/T=1, FEN=1, PFEN=1, CEN=1 and SI=0, which triggers the compaction mode of IET-MISR registers. Then the test pattern generator is activated and the network of interconnections is stimulated with a sequence of tests designed to detect faults within the network. Simultaneously, IET-MISR registers perform compaction of responses to the sequence of test vectors. After t_{det} clock periods, where t_{det} stands for duration of the detection tests, the IET-MISR registers in all COMP modules and the IET-MISR register in the PCOMP module contain so called intermediate signatures. Next, the levels of the CEN and SIG signals are changed to CEN=0 and SIG=1 and the IET-MISR registers are allowed to keep running for further $(B-1) \cdot n$ clock periods. It is the time that is needed for the IET-MISR register in PCOMP$_B$ module to carry out time compaction of the aforementioned intermediate signatures. The final content of that register makes up the *n*-bit signature $\boldsymbol{s_d}$ for the fault detection test and the signature is evacuated into an external tester. Should the $\boldsymbol{s_d}$ signature is correct the test process for the network of interconnections is finished. Otherwise the MISR registers in all COMP modules and in the PCOMP module are filled with nulls and the 00..01 vector (made up of z $n-1$ zeros and a single logic '1') is shifted into each CSR register. Simultaneously, the test pattern generator is loaded with the initial vector of the test sequence designed for localization of faults.

To make the total testing time shorter the *n* initial clock periods assigned to load new settings into MISR and CSR registers and into the test pattern generator can be parallelized with evacuation of the $\boldsymbol{s_d}$ signature into an external tester.

Step 6: localization of faults on interconnection lines

Controls signals must be set accordingly to enable the IET-MISR registers to independently compact responses received from the network of interconnections, i.e. SIG=0, D/T=1, FEN=1, PFEN=1 and CEN=1. Then the *n* cycles of tests for localization and identification of faults in interconnections are carried out where t_{loc} clock periods of each test cycle, where $= 0, 1, \ldots, n$-1, are devoted to deliver a sequence of dedicated fault-localization test vectors to inputs of the network under test. It is also the time when IET-MISR registers are employed for compaction of test response sequences received from outputs of interconnection lines connected to inputs number j of these registers. Upon the compaction process is finished the signatures formed in IET-MISR registers are serially shifted out into an external tester and converted by an external tester into normalized signatures with comparison against corresponding normalized reference signatures. Should any discrepancies between current and reference signatures are revealed the specific interconnection if qualified as a defective one. In parallel, the IET-MISR registers are filled with all-null strings. Next, the content of the CSR register is shifted by one position with SCI=0, which makes it possible to carry out the next testing cycle when IET-MISR registers shall perform compaction of test response sequences received from interconnection lines connected to inputs number $j + 1$ of these registers.

Step 7: identification of static faults

Normalized signatures corresponding to defective interconnections are compared against normalized signatures collected for all-one and all-zero sequences, which makes it possible to identify such faults as stuck-at-1 and stuck-at-0 faults of interconnection lines. However, if the stuck-at-1 (stuck-at-0) faults are not identified the normalized signatures for defective lines are mutually compared one against another. Each pair of two identical signatures indicate the lines that are shorted one to another. However, normalized signatures of shorted lines must be also compared against normalized reference signatures for all interconnections. Successful result of the comparison indicates a strong driver short (SDS fault). All other faults that could not be identified during this step as a stuck-at-level (1 or 0) or as a short shall be considered as dynamic faults. Should the latter are missing the diagnostic process for a network of interconnections is terminated.

Step 8: diagnostics of dynamic faults

For any interconnection that exhibits a dynamic fault and, in consequence, its response to a test sequence is to be determined, one has to carry out the following procedure:

- serial shifting of relevant masking vectors into CSR registers of COMP and PCOMP modules,
- serial shifting of a vector corresponding to the primitive polynomial $p_1(x)$ into the PSR register of the PCOMP module;
- setting of the following levels for control signals: SIG = =MEN = CEN = D/T = FEN = PFEN =0;
- clearing content of MISR registers in COMP and PCOMP modules during subsequent *n* clock periods;
- change of settings for control signals: SIG=PFEN=CEN=1, FEN=MEN=D/T=0;
- supplying of a test sequence vectors to inputs of the interconnection network, which takes subsequent *m* clock periods;
- change of settings for control signals: SIG=1, PFEN=CEN=FEN=MEN=D/T=0;
- serial evacuation of the $\boldsymbol{s_1}$ signature from the PCOMP module to an external tester, it takes *n* clock periods;
- in case of an interconnection line connected to the j^{th} input of the l^{th} COMP module a test response fragment with the length of ρ bits is evacuated to an external tester, which needs ρ clock periods;
- change of settings for control signals: SIG=MEN=CEN=D/T=FEN=PFEN=0;

- clearing of MISR registers in COMP and PCOMP modules during subsequent *n* clock periods;
- execution of the following operations for $i = 2, 3, \ldots, k'$:
  - serial filling of the PSR register in the PCOMP module with a vector that corresponds to a subsequent primitive polynomial $p_i(x)$;
  - change of settings for control signals: SIG=PFEN=CEN=1, FEN=MEN=D/T=0;
  - delivering of a test sequence to inputs of the interconnection network during *m* consecutive clock periods;
  - change of settings for control signals: SIG=1, PFEN=CEN=FEN=MEN=D/T=0;
  - serial evacuation of the signature $\boldsymbol{s_i}$ collected in the PMISR register of the PCOMP module into an external tester, the operation needs *n* clock periods;
- use of the set of k' signatures obtained from subsequent tests to establish the final tests response $\boldsymbol{w}$ for the interconnection under test.

Comparison of the final sequence $\boldsymbol{w}$ received from tests against the test sequence delivered to input of the interconnection line under test makes it possible to draw conclusions with regard to the nature and possible scope of dynamic faults affecting the interconnection. ♦

VI. RECAPITULATION

This study is a follow-up of investigations initiated in [12] and is meant to disclose an innovative method capable of supporting the analysis of reasons for possible dynamic faults that may disturb interconnections between digital cores of systems on chips. The method assumes that the set of collected signatures is then used for reproduction of test response sequences for defective interconnections, which facilitates identification of dynamic fault types. The approach presented here and dedicated to diagnostics of faults in interconnections is an extension of the method already disclosed in [11], since that method is limited to merely static faults.

Number of signatures that have to be collected according to the method described in this study is directly proportional to the length of the response to the test for the interconnection line, i.e. also to the length of test sequence delivered to the line input. Nevertheless, that number is irrelevant to the number of faults detected by the specific test sequence. It is the feature that is an advantage of the method as compared to the solution described in [20] that needs the number of signatures that is proportional to the number of incorrect bits in strings to be read from scan paths (in practice, the number of signatures collected should be at least twice higher than the number of faults). The above relation is illustrated by means of the graph in Fig. 8 that shows the number of *n*-bit signatures to be collected as a function of the number of faults occurring in a *m*-bit sequence of test response. The dashed line and the solid line depict the mentioned relationship respectively for the method disclosed in [20] and for the solution described in this study.

The graphs exhibit that the number of signatures that are necessary to find out the test response sequence by means of the method disclosed in [20] increases linearly in pace with the number of faults in the test response sequence. Thus, the solution is no longer efficient when the number of faults is

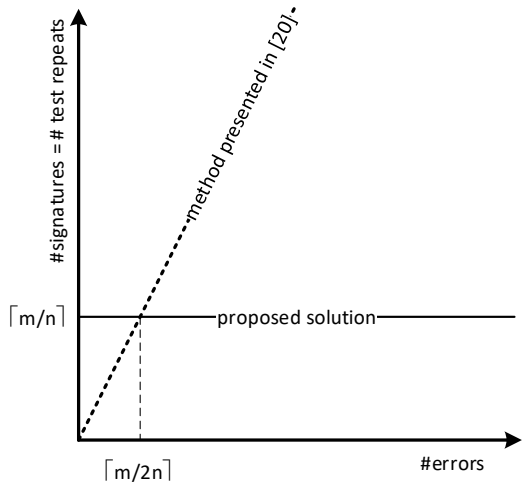

Fig. 8. Graphs illustrating the relationship between the number of *n*-bit signatures, which are necessary to determine *m*-bit sequence of the test response and the number of errors in that sequence; the graphs are presented for the method developed in [20] and the solution disclosed in [12] and in this article

really large since a huge number of signatures must be collected and processed. On the contrary, the method presented in this study is free of that drawback as the number of signatures to be found out remains constant and equals to $\left\lceil \frac{m}{n} \right\rceil$, regardless the number of faults in the test response sequence. In practice, the method disclosed herein is worse than the solution from [20], i.e. needs more signatures to be collected only when relatively small number of faults, less than $\left\lceil \frac{m}{2n} \right\rceil$, occurs in the network of interconnections.

Another substantial advantage of the method presented herein consists in its flexibility. It imposes no constrains either to the number of lines in the network of interconnections under test, or to its topology, or to the type of test pattern generator to be applied. The practical implementation of the suggested methods offers a really broad spectrum of possible solutions that differ from each other by the number of PCOMP modules incorporated into the IBIST structure. Each of such solutions needs a different hardware redundancy and time that is necessary to identify dynamic faults in interconnections, consequently a reasonable balance can be found between these parameters. The foregoing issues are addressed in this study much more thoroughly than in case of [12].

Since linear registers (MISRs) employed for compaction of test response sequences are operated at high clock frequency, the method disclosed herein enables high level of diagnostic resolution. Test response sequences are recorded at the rated speed of the system operation but they can be evacuated to an external tester at much lower frequencies. In addition, the analysis covers the entire test response sequence for the interconnection under test, which leads to formation of the final signature available from the PMISR register of the PCOMP module. The timeframe for the test response analyzer can be controlled in a rather simple way, just as typically for circuits with embedded self-testing BIST hardware.

Another undeniable advantage of the method presented herein is also the possibility to have the test response sequence for the interconnection in question determined with enhanced dependability. For that purpose one has to adhere to the

content of Conclusion 4 and carry out one more measurement for the test response sequence in order to record the $(k+1)^{th}$ signature. Should the sequences calculated for each k-component subset of the set of $k+1$ signatures are found identical one can assume that the calculated sequence is the actual response to the tests applied to the interconnection in question. Otherwise all $k+1$ measurements for the investigated test response sequence must be repeated.

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